VEGA Single Board Computer

COM Express Form-factor Embedded Computer with Configurable COM Express CPU and Integrated Data Acquisition

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IMPORTANT SAFE-HANDLING INFORMATION

- **WARNING!**
- **ESD-Sensitive Electronic Equipment.**
- **Observe ESD-safe handling procedures when working with this product.**
- **Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.**
- **Always store this product in ESD-protective packaging when not in use.**

Safe Handling Precautions

Vega contains numerous I/O connectors that connect to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor's) embedded computer boards.

ESD damage — This type of damage is almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board simply stops working because some component becomes defective. Usually the failure can be identified and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage during handling or storage — On some boards, we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However, these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However, our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

Power supply wired backwards — Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply. In this case the board will most likely will be unrepairable and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. **Check twice before applying power!**

Board not installed properly in PC/104 stack — A common error is to install a PC/104 board accidentally shifted by 1 row or 1 column. If the board is installed incorrectly, it is possible for power and ground signals on the bus to make contact with the wrong pins on the board, which can damage the board. For example, this can damage components attached to the data bus, because it puts the ±12V power supply lines directly on data bus lines.

Overvoltage on analog input — If a voltage applied to an analog input exceeds the design specification of the board, the input multiplexor and/or parts behind it can be damaged. Most of our boards will withstand an erroneous connection of up to ±35V on the analog inputs, even when the board is powered off, but not all boards, and not in all conditions.

Overvoltage on analog output — If an analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most of our boards, a short circuit to ground on an analog output will not cause trouble.

Overvoltage on digital I/O line — The digital circuitry can be damaged if a digital I/O signal is connected to a voltage above the Vega's maximum specified voltage. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and the damage could even extend past that chip to others in the circuit.

Bent connector pins — This type of problem is often only a cosmetic issue and is easily fixed by bending the pins back to their proper shape one at a time with needle-nose pliers. The most common cause of bent connector pins is when a PC/104 board is pulled off the stack by rocking it back and forth left to right, from one end of the connector to the other. As the board is rocked back and forth it pulls out suddenly, and the pins at the end get bent significantly. The same situation can occur when pulling a ribbon cable off of a pin header. If the pins are bent too severely, bending them back can cause them to weaken unacceptably or even break, and the connector must be replaced.

1. INTRODUCTION

Vega is an embedded single board computer in the COM Express form factor that mates an off-the-shelf COM Express COM CPU with an I/O baseboard that provides a wealth of PC I/O, a complete data acquisition sub-system, and a DC/DC power supply.

Vega's core embedded-PC functionality is implemented with a COM Express CPU module mounted on the bottom side of an I/O baseboard. This approach results in several benefits including enhanced thermal management, increased space for I/O functions and interface connectors, and scalable processing power. Accordingly, Vega integrates the equivalent functions of five embedded boards — CPU, system I/O, industry-leading data acquisition, Gigabit Ethernet, and a wide-input DC-to-DC power supply — all within the compact and modularly-expandable EMX Basic single board computer form-factor.

Thanks to Vega's modular architecture, you can select from a wide range of COM Express-based CPUs to meet each application's specific performance, power, and cost requirements. Available processors include an Intel 2.1GHz Core i7 and 1.4GHz Celeron CPU. What's more, Vega's on-board EMX stack location facilitates the addition of both custom and off-the-shelf I/O expansion modules to tune system functionality to the application's precise requirements.

Vega is offered in a range of models that vary according to the choice of COM Express CPU module, on-board SO-DIMM SDRAM capacity, variable-input DC/DC supply, and optional data acquisition circuitry.

1.1 Key Features

Vega's extensive set of features derives from functions present on the Vega I/O baseboard plus additional functions provided by the attached COM Express computer-on-module (COM) macrocomponent. Both are summarized below.

1.1.1 COM Express Computer-on-Module (COM) Features

Processor: Choice of Intel® 2.1GHz Core i7-3612QE, 1.7GHz Core i7-3517UE, or 1.4GHz Celeron 827E CPU
RAM: 200-pin SO-DIMM socket; supports up to 8GB DDR3 SDRAM
Graphics:

- Integrated Intel HD Graphics 3000
- Supports dual independent displays
- VGA CRT interface up to 2048 x 1536 at 60Hz
- LCD flat panel interface (LVDS); provides LCD backlight control signals
- DisplayPort

Audio: HD audio Realtek ALC262 CODEC on I/O baseboard; mic in, stereo in/out signals
Mass storage: 1 SATA interface
Ethernet interface: 1 10/100/1000Mbps port (magnetics provided on I/O baseboard)
USB: 4 USB 2.0 ports
Other: SMB, LPC, PCIe
COM Express, Type II compliant form-factor (physical and electrical)

1.1.2 Vega Baseboard Features

Additional Ethernet interface: 10/100/1000Base-T port
4 RS-232/422/285 serial ports supporting TX, RX, RTS and CTS
Industry-leading data acquisition subsystem (available on A models only):

- 16 16-bit A/D inputs usable as: 16 single-ended / 8 differential
- 100KHz maximum aggregate sampling rate for gains 4 and 8
- 250KHz maximum aggregate sampling rate for gains below 4
- Programmable input ranges: +/-10V, +/-5V, +/-2.5V, +/-1.25V, 0-10V, 0-5V, 0-2.5V
- 2048 A/D FIFO
- 8 16-bit D/A channels
- +/-10V and 0-10V output ranges
- 30 programmable bidirectional digital I/O lines with 3.3V logic, arranged in three groups of 8 signals
- 4 24-bit pulse width modulators
- 8-channel waveform generator
- 8 32-bit counter/timers
- On-board EEPROM storage of auto-calibration values

Status LEDs:

- Power LED
- Ethernet link and speed LEDs

- COM Express socket on bottom; conforms to COM Express v3.0 specification
- I/O connectors provided for all I/O
- mSATA and USB flashdisk socket supports up to 64GB
- PCIe MiniCard socket
- EMX I/O stackable expansion
- Built-in DC/DC power supply:
  - Input voltage: +7V to +36V DC/DC power supply
  - Power consumption: VEGA-3612QE-4GA -- 14.52W at 12V typical
VEGA-3517UE-4GA -- 13.93W at 12V typical
VEGA-827E-2GA -- 14.7W at 12V typical
  - Output voltages: +5V, +3.3V
  - Switched outputs: +5V, +12V, +3.3V
- Operating temperature: -40°C to +85°C
- Operating humidity: 5% to 95% non-condensing
- Form-factor:
  - 4.92 x 3.74 inches (125 x 95 mm)
  - COM Express dimensions and mounting holes

1.2 Operating System Compatibility

Vega's operating system compatibility depends on both the Vega baseboard and the specific COM Express CPU module attached to it. The baseboard has been qualified for use with the following operating systems:

- Windows Embedded Standard 7, Windows Embedded CE
- Linux v2.6.23

The operating systems supported by the COM Express CPU module vary according to the specific COM Express module used. Consult the appropriate COM Express CPU module's user manual for details on its operating system support.

1.3 Vega SBC Models

Several models of the Vega SBC are available with different COM Express CPU modules, memory, and optional on-board data acquisition circuitry. These models are described in the following table.

Model Number	Description
VEGA-3612QE-8GA	Vega SBC, 2.1GHz Intel Core i7-3612QE CPU, 8GB RAM, full data acquisition
VEGA-3612QE-8GN	Vega SBC, 2.1GHz Intel Core i7-3612QE CPU, 8GB RAM, no data acquisition
VEGA-3612QE-4GA	Vega SBC, 2.1GHz Intel Core i7-3612QE CPU, 4GB RAM, full data acquisition
VEGA-3612QE-4GN	Vega SBC, 2.1GHz Intel Core i7-3612QE CPU, 4GB RAM, no data acquisition
VEGA-3517UE-4GA	Vega SBC, 1.7GHz Intel Core i7-3517UE CPU, 4GB RAM, full data acquisition
VEGA-3517UE-4GN	Vega SBC, 1.7GHz Intel Core i7-3517UE CPU, 4GB RAM, no data acquisition
VEGA-827E-2GA	Vega SBC, 1.4GHz Intel Celeron 827E CPU, 2GB RAM, full data acquisition
VEGA-827E-2GN	Vega SBC, 1.4GHz Intel Celeron 827E CPU, 2GB RAM, no data acquisition

1.4 Thermal Considerations and Heatspreader

All models of Vega are specified for an operating temperature range of -40°C to +85°C. Diamond Systems provides a heatspreader attached to the Vega SBC as a conductive cooled thermal layer. However, this heatspreader by itself does not constitute the complete thermal solution necessary for any specific implementation, but provides a common interface between the single board computer and the customer's implementation-specific thermal solution.

The outside surface of the Vega heatspreader must be kept at a temperature not to exceed +85°C. If your environment causes the temperature on the outside surface of the heatspreader to exceed the appropriate temperature, you are responsible for removing the additional heat from the system through either an additional passive thermal solution or fan solution.

Vega's integrated heatspreader makes thermal contact with the heat generating components and provides a flat surface on the bottom of the assembly for mating to the system enclosure. This technique facilitates efficient removal of heat from the COM module without the need for a fan. Four mounting holes on the bottom of the conduction cooled heatspreader are provided to mount Vega in an enclosure or to a bulkhead. These mounting holes are #6-32 threaded holes on 2.8" centers.

1.5 Cable Kit

The Vega cable kit (part number (CK-VEGA-01) provides convenient access to all of Vega's I/O features. The kit's cables are shown in the photo below and are identified in the table that follows.

The components of the Vega Cable Kit are listed below.

Item	*Qty*	*Diamond P/N*	*Description*	*Connects to…*
1	2	6980808	Dual serial cable	J14, J15
2	1	6981501	Utility cable	J19
3	1	6981503	Power input cable	J29
4	2	6981504	Data acquisition cable	J8, J10
5	2	6981315	Gigabit Ethernet cable	J11, J12
6	2	6981317	Dual USB cable	J17, J18
7	1	6981323	HD audio cable	J22
8	1	6981324	VGA cable	J28

2. FUNCTIONAL OVERVIEW

2.1 Block Diagrams

Figure 1 shows the functional blocks of the Vega I/O baseboard. As indicated in the block diagram, the baseboard circuitry primarily comprises the data acquisition subsystem, Gigabit Ethernet controller, DC/DC power supply, and I/O interfaces. The COM Express module integrates to the I/O baseboard via connectors A/B and C/D and provides the system's core embedded PC functionality.

Although COM Express CPU module processors and precise functions vary between specific modules, the block diagram of a typical COM Express CPU module is shown in Figure 2.

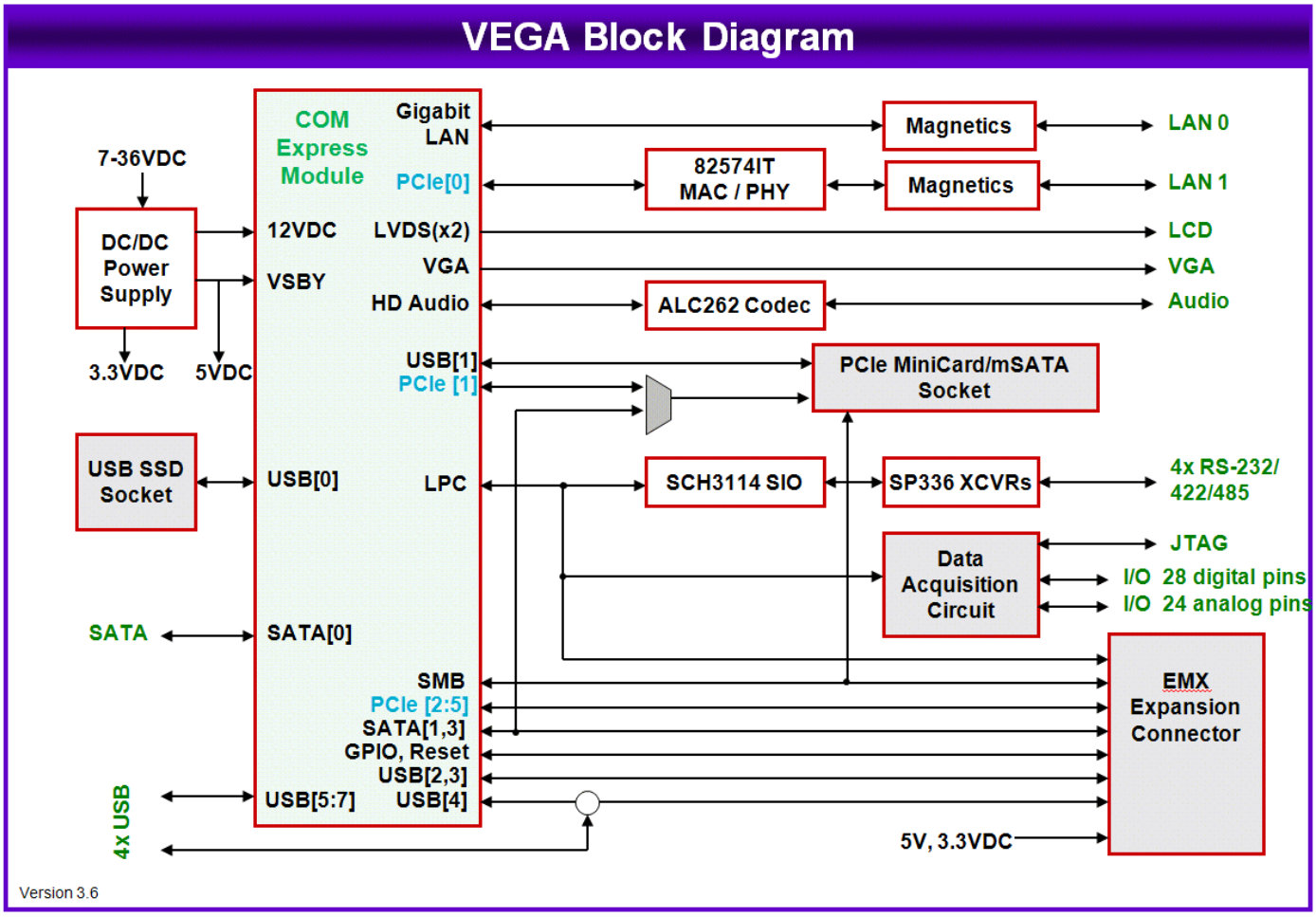


Figure 1: Vega I/O Baseboard Functional Block Diagram

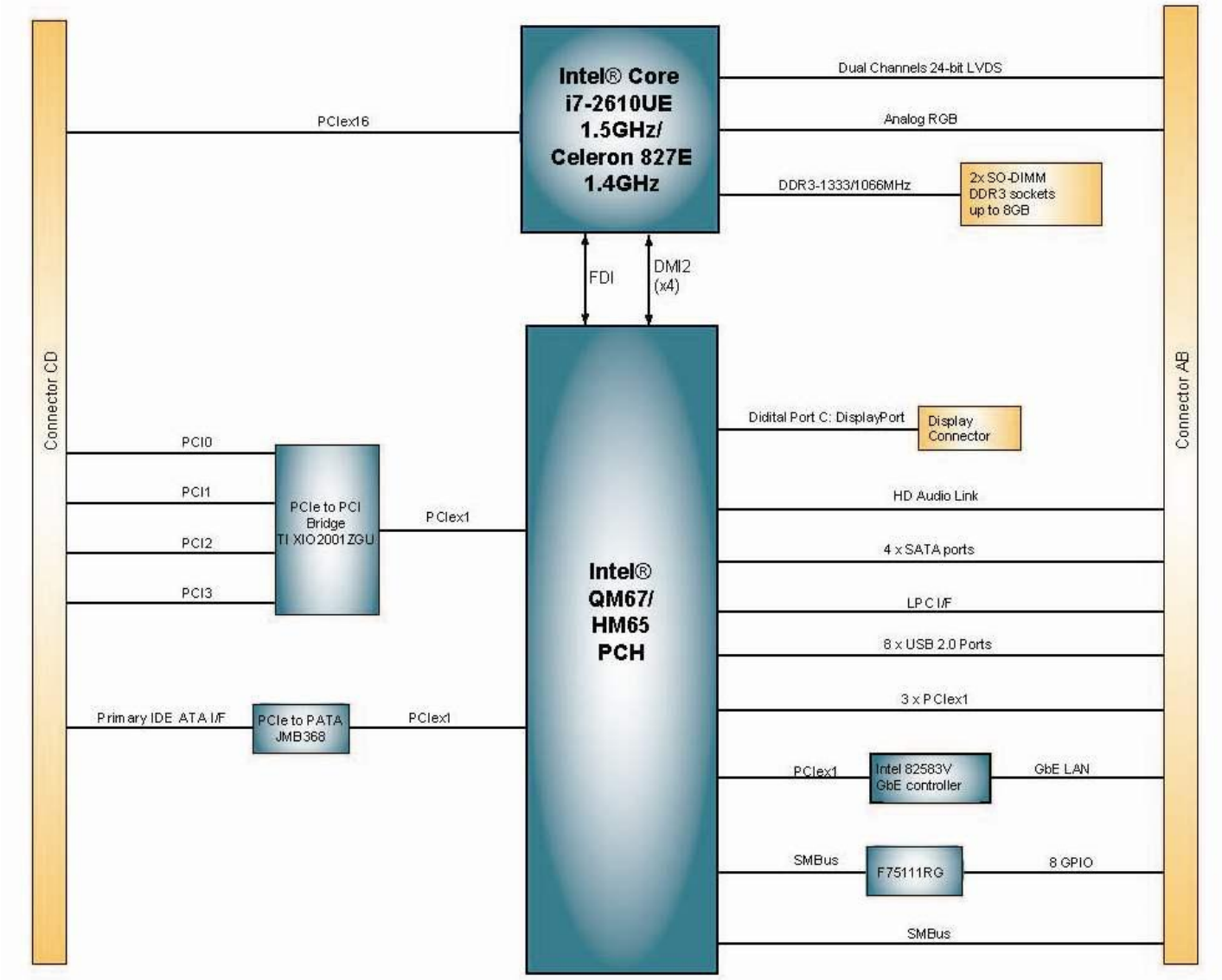


Figure 2: Typical COM Express CPU Module Functional Block Diagram

2.2 Functional Overview

This section describes the major Vega subsystem.

2.2.1 CPU Core

Vega's core embedded computer is based on a COM Express CPU offering a choice of an Intel® 2.1GHz Core i7-3612QE or 1.4GHz Celeron 827E CPU. The COM Express COM module provides the standard PC I/O for the Vega system as described in the following sections.

2.2.2 Video

The VGA and LVDS signals from the COM Express connector are connected to on-board connectors. LCD power may be jumper-selected for +3.3VDC or +5VDC. Backlight power may be jumper-selected for +5VDC or +12VDC. Both voltages are generated on-board. Several of the PEG pins from the second (C/D) COM Express connector are routed to a connector that can be used to attach a daughter card to the EMX Baseboard.

2.2.3 Ethernet

Vega provides an Intel 82574IT Gigabit Ethernet Controller attached to the first x1 PCI express lane on the processor. The board also includes the magnetics to support the 82574IT controller and the Gigabit LAN interface from the COM Express CPU.

2.2.4 USB

Vega offers four user accessible USB 2.0 ports. All ports have minimum 500mA per port drive capability with short circuit / over current and ESD protection on each port. Ports 1-4 are brought out to I/O connectors for user access. A separate USB connector is provided for mounting a solid state bootable USB flashdisk module with capacity up to 8GB.

2.2.5 Serial Ports

Vega provides four serial ports with full RS-232/422/485 protocol support and TX, RX, RTS and CTS signal availability. The SCH3114 provides maximum data rates of 460.8k. Jumper configurable 120-ohm termination resistors are available for RS-485 mode.

2.2.6 High Definition Audio

The high definition Audio signals from the COM Express attached processor are connected to the ALC262 HD-Audio Codec. The ALC262 will support Stereo Line-in, Stereo Line-out and Mono MIC on an on-board connector.

2.2.7 Data Acquisition

The board provides the following data acquisition capabilities.

Type of I/O	*Characteristics*
Analog Input	16 single-ended/8 differential inputs, 16-bit resolution 250KHz maximum aggregate A/D sampling rate for gains below 4 100KHz maximum aggreagte A/D sampling rate for gains 4 and 8 Programmable input ranges/gains: +/-10V, +/-5V, +/-2.5V, +/-1.25V, 0-10V, 0-5V, 0-2.5V 2048 sample A/D FIFO for reliable high-speed sampling
Analog Output	8 analog outputs, 16-bit resolution ±10V and 0-10V output ranges Indefinite short circuit protection on outputs
Digital I/O	30 programmable digital I/O, 3.3V logic compatible
Counter/Timers	One 32-bit counter/timer for A/D sampling rate control One 16-bit counter/timer for user counting and timing functions

On board I^2C flash EEROM is provided for auto-calibration value storage.

2.2.8 I/O Expansion

The Vega baseboard supports a standard PCIe MiniCard socket. It uses the x1 PCIe (Port 1) from the COM Express attached processor. One of the USB ports (Port 1) from the COM Express connector is terminated to the PCIe MiniCard socket. This may be used to plug-in WiFi Modules and Memory devices. The PCIe MiniCard module is fastened to the board by means of screws and soldered spacers.

The 120 pin EMX connector provides the means for adding expansion I/O modules. The connector supports the following functions: Four PCIe x1, one PCIe x4 (not connected on the EMX Baseboard), three USB, one SATA (a second SATA for future expansion), LPC, SMBus.

2.2.9 Power Supply

The Vega baseboard provides power for both the COM Express attached processor board and the EMX I/O expansion boards. All the necessary power supply voltages are derived from a variable +7VDC to +36VDC input, using onboard discrete-design DC/DC converter circuits These supplies include the standby supplies for the COM Express connector.

2.2.10 Battery Backup

The Vega baseboard includes a backup battery for CMOS RAM backup and real-time clock for the attached processor module. A 2-pin header is provided for an external battery connection. The power for battery backup can be augmented by an expansion I/O module connected to the EMX connector.

2.3 BIOS

The AMI BIOS includes the following key features:

- Boot from LAN (PXE) and USB as well as C: and D:
- User selectable Master boot device selection
- Free boot sequence configuration
- Support for various LCD configurations supported by the video chipset
- Console (display and keyboard) redirection to serial port
- BIOS recovery through USB attached storage or other means
- Configurable default settings in battery-less configurations
- Initialize USB keyboard & mouse
- Customizable splash screen

2.3.1 BIOS Setup

The Vega COM Express CPU module's BIOS ROM provides a wide range of configuration options. When you power up the Vega SBC, you can immediately enter the BIOS "Setup" utility (prior to OS boot-up) in order to adjust BIOS settings to match your system's peripheral devices and other requirements, and to configure various other hardware and software parameters.

Options configurable via Setup typically include:

Number and type of mass storage devices
Boot device priority
Video display type and resolution
SATA, serial, and parallel interface modes and protocols
PCI and PnP configuration
Power management setup
Automatic power-up after LAN connection, RTC alarm, power resumption, etc.
System monitoring and security functions

The precise configuration options available via the BIOS Setup utility — and the specific keystroke sequence required to launch Setup on power-up — vary according to the specific COM Express CPU module attached to the Vega baseboard. Refer to the COM Express CPU module's user manual for further details.

2.4 Board Layout

Figure 3 illustrates the location of connectors and jumpers on the top side of the Vega I/O baseboard. Figure 4 illustrates the location of connectors on the COM Express CPU. The COM Express CPU module attaches on the baseboard's bottom side.

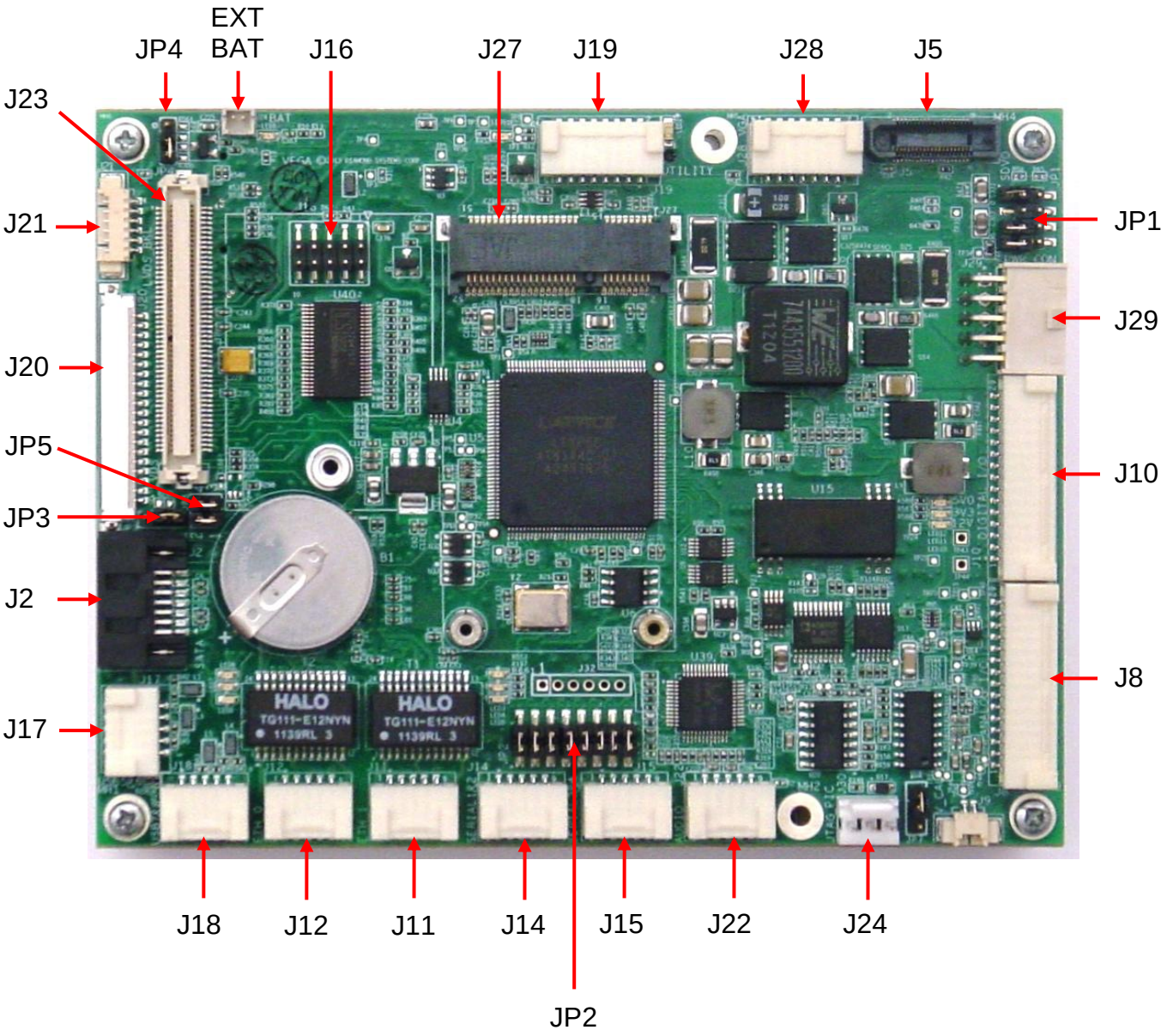


Figure 3: Vega I/O Baseboard Top View

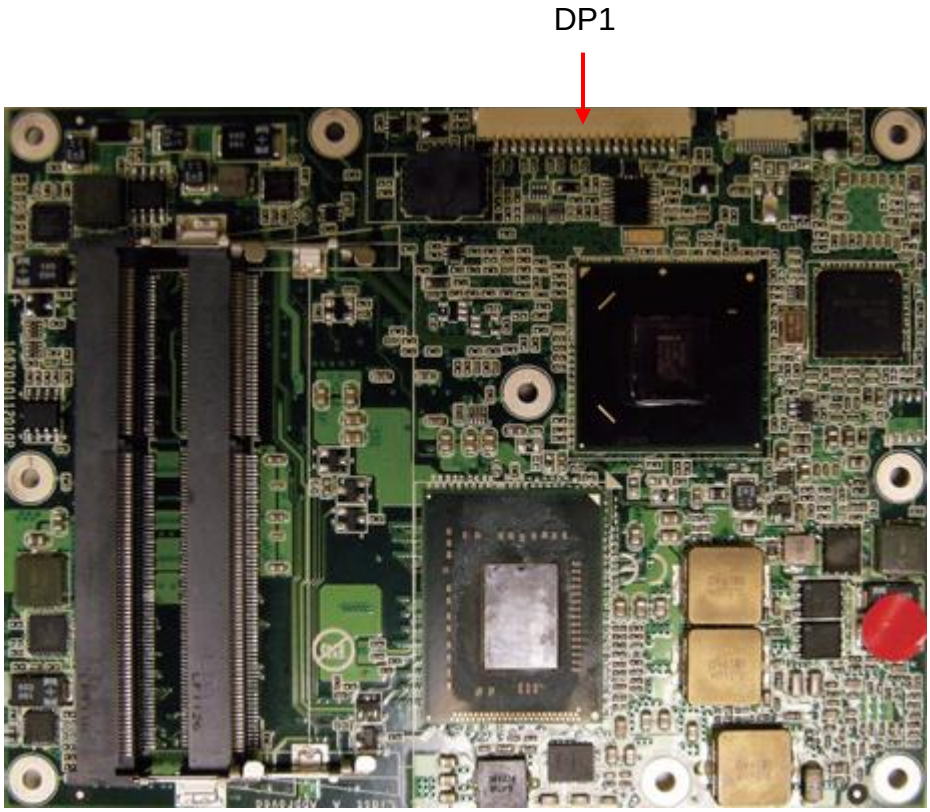


Figure 4: COM Express CPU Bottom View

2.5 Interface Connector Summary

The table below summarizes the functions of Vega's interface, utility, and power connectors. The table also identifies which major subsystem — COM Express CPU module or Vega I/O baseboard — provides the electronics associated with each connector.

Signal functions relating to all of Vega's interfaces connectors are discussed in greater detail in Section 6.

Interface Function	*Connector Designation*	*Associated Subsystem*	*Supported by Cable Kit*
SATA	J2	COM Express CPU module	No
LCD2 LVDS Interface	J5	Vega baseboard	No
Analog I/O	J8	Vega baseboard	Yes
Digital I/O	J10	Vega baseboard	Yes
Gigabit Ethernet Port 1	J11	Vega baseboard	Yes
Gigabit Ethernet Port 0	J12	COM Express CPU module	Yes
Serial Ports COM1-COM4	J14, J15	Vega baseboard	Yes
USB Flashdisk	J16	Vega baseboard	No
USB 2.0	J17, J18	COM Express CPU module	Yes
Utility Signals	J19	Vega baseboard	Yes
LCD1 LVDS Interface	J20	COM Express CPU module	No
LCD Backlight	J21	COM Express CPU module	No
Audio	J22	Vega baseboard	Yes
EMX I/O expansion	J23	Vega baseboard	No
External Battery	J24	Vega baseboard	No
PCIe MiniCard/mSATA socket	J27	Vega baseboard	No
VGA Display	J28	COM Express CPU module	Yes
Input Power	J29	Vega baseboard	Yes
External battery	EXT BAT	Vega baseboard	No
Display Port	DP1	COM Express CPU	No

Note: *COM Express COM I/O functions vary according to the specific COM Express module that is attached to the Vega baseboard. For further details on functions listed above that are generated by the COM Express CPU module, consult the specific COM Express CPU module's user manual.*

2.6 Configuration Jumper Summary

The Vega baseboard's configuration jumper blocks are listed below. Details regarding the use of these jumpers appear in Section 5 of this document.

Jumper	*Description*
JP1	Digital I/O output resistors and FPGA base address
JP2	RS-422/485 termination resistors
JP3	LCD supply voltage
JP4	LCD backlight power
JP5	LCD panel scan direction and map setting

3. INTERFACE CONNECTOR DETAILS

This section describes functions associated with the Vega I/O baseboard's EMX bus expansion stack, utility, and power interface connectors in greater detail. Refer to Section 3 of this document for information regarding mating cable assemblies that are provided in the Vega Cable Kit.

3.1 SATA (J2)

The SATA connector is an industry-standard right-angle connector. It is mounted flush with the edge of the board so that a standard SATA cable can be used to connect the board to an external hard drive.

3.2 LCD2 LVDS Interface (J5)

J5 is a second LCD connector to support dual channel LCD panels.

D3+	**1**	**2**	D2+
D3-	**3**	**4**	D2-
Signal Gnd	**5**	**6**	Signal Gnd
D1+	**7**	**8**	D0+
D1-	**9**	**10**	D0-
Signal Gnd	**11**	**12**	Signal Gnd
Clock+	**13**	**14**	VLCD
Clock-	**15**	**16**	VLCD
Power Gnd	**17**	**18**	Power Gnd
DDC Data	**19**	**20**	DDC Clock

Connector description: JST SM20B-GHDS-G-TF 2x10 right angle 1.25mm pitch gold
Connector part number: JST GHDR-20V-S

3.3 Analog I/O (J8)

Connector J8 provides the analog I/O signals from the on-board data acquisition circuitry. There are no ESD protection diodes for these signals. This funtionality is only available on Vega A models.

VIN0	1	2	VIN8
VIN1	3	4	VIN9
VIN2	5	6	VIN10
VIN3	7	8	VIN11
VIN4	9	10	VIN12
VIN5	11	12	VIN13
VIN6	13	14	VIN14
VIN7	15	16	VIN15
AGND_DAQ	17	18	AGND_DAQ
VOUT0	19	20	VOUT1
VOUT2	21	22	VOUT3
VOUT4	23	24	VOUT5
VOUT6	25	26	VOUT7
AUX_IO0R	27	28	AUX_IO1R
EXTRIGR	29	30	GND

Connector description: CONN,2x15P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM30B-ZPDSS-TF

3.4 Digital I/O (J10)

Connector J10 provides the digital I/O signals from the on-board data acquisition circuitry. These signals originate with the FPGA and have ESD protection diodes. The digital I/O is organized in four groups (A, B, C, and D). Ports A, B and C have eight signals each and Port D consists of 6 signals. Ports C and D also offer special counter/timer, pulse width modulator, and waveform generator functions.

PA0R	1	2	PA1R
PA2R	3	4	PA3R
PA4R	5	6	PA5R
PA6R	7	8	PA7R
PB0R	9	10	PB1R
PB2R	11	12	PB3R
PB4R	13	14	PB5R
PB6R	15	16	PB7R
PC0R	17	18	PC1R
PC2R	19	20	PC3R
PC4R	21	22	PC5R
PC6R	23	24	PC7R
AUX_IO2R	25	26	AUX_IO3R
TOUT0R	27	28	GND
+5V	29	30	GND

Connector description: CONN,2x15P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM30B-ZPDSS-TF

3.5 Gigabit Ethernet (J11, J12)

The Vega SBC provides two Gigabit Ethernet ports, one provided directly from the COM Express COM CPU (J12) and the other generated on the Vega I/O baseboard (J11). The connector pinout for both ports is identical.

DA+	1	2	DB+
DA-	3	4	DB-
DC+	5	6	DD+
DC-	7	8	DD-
CGND	9	10	NC

Connector description: CONN,2x5P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM10B-ZPDSS-TF

3.6 Serial Ports (J14, J15)

The Vega I/O baseboard provides four serial ports on two pin headers, two ports on each. Connector J14 provides signals for Port 1 and Port 2. Connector J15 provides signals for Port 3 and Port 4.

All four ports support RS-232/422/485 multiprotocol with the TX, RX, RTS and CTS signals. The connector pinout for both ports is identical.

Protocol / Port#	RS-232				RS-422 Full Duplex				RS-485 Half Duplex			
Port 1	TX1	1	2	RX1	TX1+	1	2	RX1+	TX1+/RX1+	1	2	NC
	GND	3	4	GND	GND	3	4	GND	GND	3	4	GND
	RTS1	5	6	CTS1	TX1-	5	6	RX1-	TX1-/RX1-	5	6	TX2-/RX2-
Port 2	CTS2	7	8	RTS2	RX2-	7	8	TX2-	NC	7	8	NC
	RX2	9	10	TX2	RX2+	9	10	TX2+	NC	9	10	TX2+/RX2+
Port 3	TX3	1	2	RX3	TX3+	1	2	RX3+	TX3+/RX3+	1	2	NC
	GND	3	4	GND	GND	3	4	GND	GND	3	4	GND
	RTS3	5	6	CTS3	TX3-	5	6	RX3-	TX3-/RX3-	5	6	TX4-/RX4-
Port 4	CTS4	7	8	RTS4	RX4-	7	8	TX4-	NC	7	8	NC
	RX4	9	10	TX4	RX4+	9	10	TX4+	NC	9	10	TX4+/RX4+

Connector description: CONN,2x5P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM10B-ZPDSS-TF

3.7 USB Flashdisk (J16)

Connector J16 hosts an on-board USB flashdisk. This is a dedicated USB port.

+5V	1	2	NC
USB0 Data-	3	4	NC
USB0 Data+	5	6	NC
GND	7	8	NC
KEY	9	10	NC

Connector description: CONN HEADER 2MM DUAL SMD 10POS

Connector part number: Sullins, NRPN052MAMS-RC

3.8 USB (J17, J18)

Connectors J17 and J18 provide access to Vega's four USB 2.0 ports. Connector J17 has USB ports 1 and 2, and connector J18 has USB ports 3 and 4. The pinout for both connectors is identical. The shield pin on each connector is tied to system ground. The pinout for connector J17 is shown below.

NC	1	2	Shield
GND	3	4	GND
USB2 Data+	5	6	USB1 Data+
USB2 Data-	7	8	USB1 Data-
USB2 Pwr	9	10	USB1 Pwr

Connector description: CONN,2x5P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM10B-ZPDSS-TF

3.9 Utility (J19)

Connector J19 provides access to Ethernet LED signals for both Ethernet ports as well as the audio speaker output.

LAN 0 LED - Activity	1	2	LAN 0 LED - Activity
3.3V	3	4	3.3V
LAN0 LED – 1000 Speed	5	6	LAN1 LED – 1000 Speed
LAN0 LED – 100 Speed	7	8	LAN1 LED – 100 Speed
GND	9	10	PWRBTN
GND	11	12	GND
SPKR	13	14	RESET
GND	15	16	GND

Connector description: CONN,2x8P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM14B-ZPDSS-TF

3.10 LCD Panel (LVDS Interface) (J20)

Connector J20 is an industry standard LVDS LCD display connector. The LCD panel power is jumper selectable for 3.3V (default) or 5V, see jumper block JP3.

1	Ground / D3+, depending on video chip
2	Ground / D3-, depending on video chip
3	Scan Direction (High = Reverse Scan, Low/short = Normal Scan)
4	LVDS Map Setting (High = Map B, Low/short = Map A)
5	LCD Ground
6	Pixel Clock +
7	Pixel Clock -
8	LCD Ground
9	D2+
10	D2-
11	LCD Ground
12	D1+
13	D1-
14	LCD Ground
15	D0+
16	D0-
17	LCD Ground
18	LCD Ground
19	Vcc 3.3V / 5V (jumper configured)
20	Vcc 3.3V / 5V (jumper configured)

Connector description: CONN,RCPT,1.25MM ,20POS,SMD,R/A

Connector part number: JAE, FI-SE20P-HFE

Cable-mount socket: JAE, FI-SE20S-2-L or equivalent

3.11 LCD Backlight (J21)

Connector J21 provides the backlight power and control for the LCD LVDS panel. If needed, +12V power must be provided on the input power connector, J29. The brightness control for the LCD backlight has a weak pull-down resistor to ensure maximum brightness when it is not connected externally.

1	Power +5V/+12V, jumper selectable; Default +5V
2	Power +5V/+12V, jumper selectable; Default +5V
3	Ground
4	Ground
5	Enable (GPIO output), 0 = off, open circuit = on
6	Brightness, 0-5VDC variable; 0V = max, 5V = min

Connector description: Hdr, 1x6 ST 1.25mm Shroud TH

Connector part number: Molex, 53261-0671

Cable-mount socket: Molex, 51021-0600 or equivalent

Terminals: Molex, 50058 / 50079 series or equivalent

3.12 Audio (J22)

Connector J22 provides the stereo line-in, stereo line-out and mono microphone signals from the ALC262 HD-Audio Codec. External speakers, headphones and a microphone can be interfaced to this connector.

LineOut – L	1	2	LineOut – R
GND_AUDIO	3	4	GND_AUDIO
LineIn – L	5	6	LineIn – R
GND_AUDIO	7	8	GND_AUDIO
MIC IN	9	10	GND_AUDIO

Connector description: CONN,2x5P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM10B-ZPDSS-TF

3.13 EMX I/O Expansion (J23)

Connector J23 allows one EMX compliant I/O expansion module to be plugged in to the Vega I/O baseboard. The connector pinout follows the EMX standard.

Gnd	1	2	Gnd	USB2+	51	52	SATA-R+
PE4T+	3	4	PE1T+	USB2-	53	54	SATA-R-
PE4T-	5	6	PE1T-	+3.3V	55	56	+3.3V
Gnd	7	8	Gnd	Reserved	57	58	Reserved
PE3T+	9	10	PE2T+	Reserved	59	60	Reserved
PE3T-	11	12	PE2T-	+5V	61	62	+5V
Gnd	13	14	Gnd	Reserved	63	64	Reserved
PE4R+	15	16	PE1R+	Reserved	65	66	Reserved
PE4R-	17	18	PE1R-	+5V	67	68	+5V
Gnd	19	20	Gnd	Reserved	69	70	SMB-Clk
PE3R+	21	22	PE2R+	Reserved	71	72	SMB-Data
PE3R-	23	24	PE2R-	+5V	73	74	SMB-Alert-
Gnd	25	26	Gnd	Reserved	75	76	+5V
PE4C+	27	28	PE1C+	Reserved	77	78	+5V
PE4C-	29	30	PE1C-	+5VSB	79	80	LPC-AD0
Gnd	31	32	Gnd	+5VSB	81	82	LPC-AD1
PE3C+	33	34	PE2C+	VBat	83	84	LPC-AD2
PE3C-	35	36	PE2C-	Wake-	85	86	LPC-AD3
+3.3V	37	38	+3.3V	IOControl1	87	88	LPC-FRAME-
PE4clkreq-	39	40	PE1clkreq-	IOControl2	89	90	LPC-SERIRQ-
PE3clkreq-	41	42	PE2clkreq-	USB-OC-	91	92	LPC-DRQ
+3.3V	43	44	+3.3V	IOReady	93	94	LPC-CLK1
USB1+	45	46	SATA-T+	Device Reset-	95	96	LPC-CLK2
USB1-	47	48	SATA-T-	Host Reset-	97	98	Gnd
+3.3V	49	50	+3.3V	Gnd	99	100	Gnd

Connector description: CONN,RCPTL,2x50,0.635mm,SMT,RH

Connector part number: MOLEX, 52901-1074

3.14 External Battery (J24)

J24 provides a connection for an external battery.

1	EXT BAT
2	GND

3.15 PCIe MiniCard / mSATA (J27)

J27 provides a shared PCIe MiniCard / mSATA socket. As a PCIe MiniCard socket, J27 accepts Diamond or third party PCIe MiniCards such as WiFi, Bluetooth, and GPS. The socket and pin out conforms to the PCIe MiniCard industry standard. As an mSATA socket, both MLC and SLC mSATA flashdisks of up to 64GB are supported.

WAKE#	1	2	+3.3V	GND	21	22	PERST#	GND	43	44	LED_WLAN#
NC	3	4	GND	PERN	23	24	+3.3V	NC	45	46	NC
NC	5	6	+1.5V	PERP	25	26	GND	NC	47	48	+1.5V
CLKREQ#	7	8	NC	GND	27	28	+1.5V	NC	49	50	GND
GND	9	10	NC	GND	29	30	SMB_CLK	NC	51	52	+3.3V
REFCLK-	11	12	NC	PETN	31	32	SMB_DATA				
REFCLK+	13	14	NC	PETP	33	34	GND				
GND	15	16	NC	GND	35	36	USB_D-				
	KEY			GND	37	38	USB_D+				
NC	17	18	GND	+3.3V	39	40	GND				
NC	19	20	W_DISABLE#	+3.3V	41	42	NC				

Connector description: CONN, PCIe MiniCard,52-P,SMT,RH

Connector part number: JAE, MM60-52B1-E1-R650

3.16 VGA (J28)

The VGA connector, J28, has the VGA signals terminated to it from the SDVO to VGA converter. A VGA monitor can be connected to this.

RED	1	2	VGA GND
GREEN	3	4	VGA GND
BLUE	5	6	VGA GND
GND	7	8	HSYNC
VSYNC	9	10	GND
DDC DATA	11	12	DDC CLK
NC	13	14	GND

Connector description: CONN,2x7P,1.5MM,LOCK,SH,R/A,SMT

Connector part number: JST, SM14B-ZPDSS-TF

3.17 Input Power (J29)

J29 is used to provide power to the Vega single board computer.

+7 to +36V	1	2	PGND
+7 to +36V	3	4	PGND
+7 to +36V	5	6	PGND
+7 to +36V	7	8	PGND
5V_STBY	9	10	PS_ON#

Connector description: CONN, 2x5pin, 2.54mm, Shroud, RA, TH

Connector part number: Samtec, IPL1-105-01-L-D-RA-K

3.18 Display Port (DP1)

Connector DP1, located on the bottom of the COM Express module, is used to provide connection to a display port compatible device.

LANE_0P	1
LANE_0N	2
GND	3
LANE_1P	4
LANE_1N	5
GND	6
LANE_2P	7
LANE_2N	8
GND	9
LANE_3P	10
LANE_3N	11
GND	12
CONF1	13
CONF2	14
AUXP	15
AUXN	16
GND	17
HPD	18
RTN_PWR	19
+3.3V PWR	20

Connector description: Industry standard display port connector

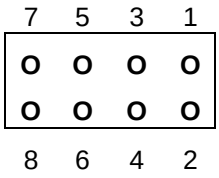
Connector part number: ACES 1.25mm 88266-200X1

4. CONFIGURATION JUMPER DETAILS

This section describes the use of the Vega I/O baseboard's configuration jumper options and indicates the default settings when appropriate.

4.1 Digital I/O Output Resistors and FPGA Base Address (JP1)

Jumper JP1 is to set the digital I/O output 10K resistors to either pull-up or pull-down. The default is no jumper, meaning neither pull-up nor pull-down is selected. Jumper JP1 also sets the FPGA base address as defined in the table below. To change the FPGA base address, first insert the desired jumper(s) and then change the BIOS to agree with the new base address. The jumper setting and BIOS setting must agree for the FPGA to function properly.



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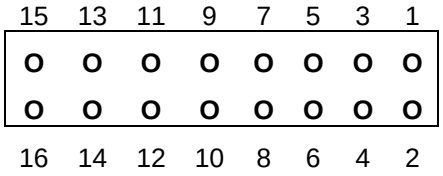
Jumper on Pins	*Jumper Function*
1 & 2	DIO 10K resistor pull up to 3.3V
3 & 4	DIO 10K resistor pull down to ground
5 & 6	FPGA base address 200
7 & 8	FPGA base address 240
5&6, 7&8	FPGA base address 280
No jumpers on 5&6 or 7&8	FPGA base address 300 (default)

Default setting: *No jumpers installed*

4.2 RS-422/485 Termination Resistors (JP2)

Jumper JP2 is used to enable termination resistors for RS-422/485 protocols on serial ports 1 through 4.

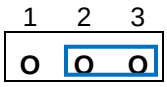


Jumper on Pins	*Jumper Function*
1 & 2	Port 1 RS-485 termination
3 & 4	Port 1 RS-422 termination
5 & 6	Port 2 RS-485 termination
7 & 8	Port 2 RS-422 termination
9 & 10	Port 3 RS-485 termination
11 & 12	Port 3 RS-422 termination
13 & 14	Port 4 RS-485 termination
15 & 16	Port 4 RS-422 termination

Default setting: *No jumpers installed*

4.3 LCD Supply Voltage (JP3)

Jumper JP3 selects the LCD panel supply voltage as either +3.3V or +5V. The default is +3.3V.



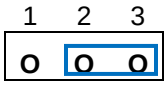
.

Jumper on Pins	*Jumper Function*
1 & 2	+5V LCD panel voltage
2 & 3	+3.3V LCD panel voltage (default)

Default setting: *Jumper on pins 2&3*

4.4 LCD Backlight Power (JP4)

Jumper JP4 selects the LCD backlight power input as either +5V or +12V. The default is +12V.



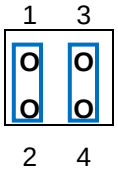
.

Jumper on Pins	*Jumper Function*
1 & 2	+5V LCD backlight power
2 & 3	+12V LCD backlight power (default)

Default setting: *Jumper on pins 2&3*

4.5 LCD Panel Scan Direction & Map Setting (JP5)

Jumper JP5 sets the LCD panel scan direction as normal or reverse scan, and the LVDS map setting as Map-A or Map-B. The default settings are normal scan and Map-A.



.

Jumper on Pins	*No Jumper*	*Jumper*
1 & 2	Reverse scan	Normal scan (default)
3 & 4	Map-B	Map-A (default)

Default setting: *Jumpers on pins 1&2, 3&4*

5. BIOS

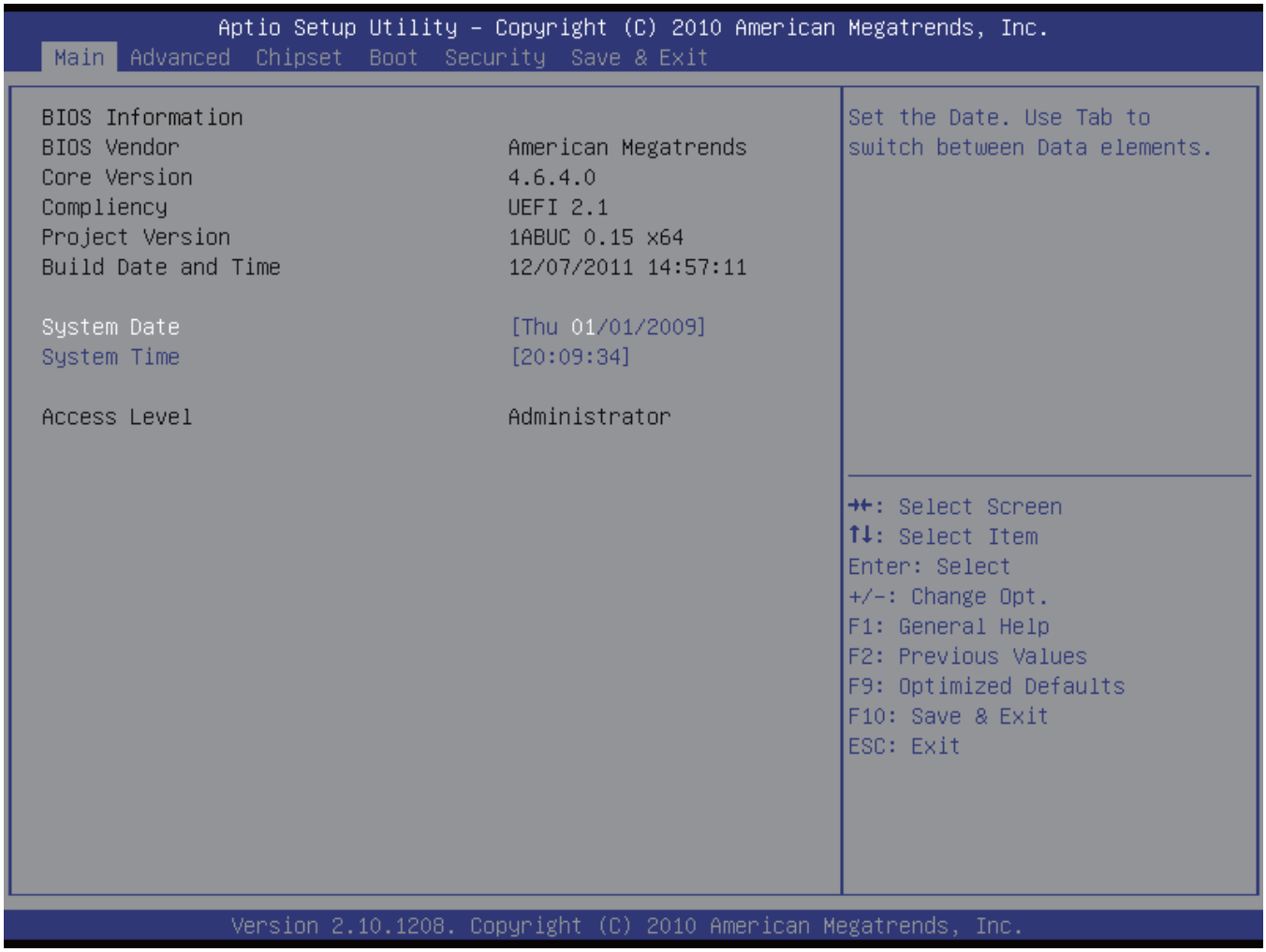
The AMI BIOS provides a setup utility program for specifying the system configurations and settings which are stored in the BIOS ROM of the system. When you power on the Vega SBC, the AMI BIOS is immediately activated. After entering the BIOS setup utility, use the left and right arrow keys to highlight a specifiic configuration screen from the top menu bar. Use the up and down arrow keys to access and configure the information in each menu. The BIOS screens in this manual are for reference only and may not exactly match what appears on the screen.

5.1 BIOS Main Setup Screen

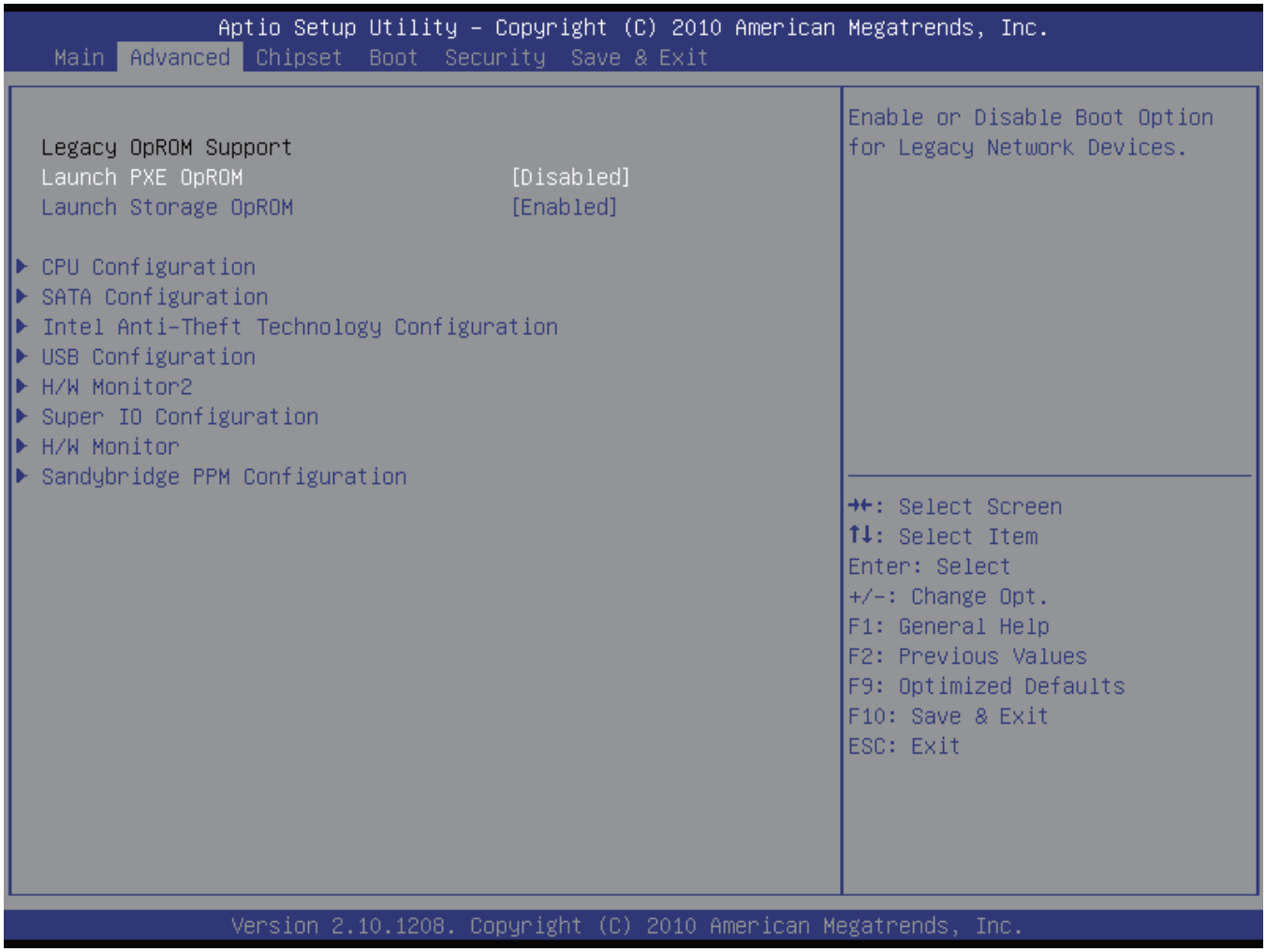
The image below shows the main BIOS setup screen. This screen provides general information about the BIOS including version number and build date.

The system date and time can be set on this screen. The Day automatically changes when the date is changed.

Configuration screens can be accessd by scrolling across the top navigation bar.


Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
BIOS Information
BIOS Vendor American Megatrends
Core Version 4.6.4.0
Compliency UEFI 2.1
Project Version 1ABUC 0.15 x64
Build Date and Time 12/07/2011 14:57:11
System Date [Thu 01/01/2009]
System Time [20:09:34]
Access Level Administrator
Set the Date. Use Tab to switch between Data elements.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit
ESC: Exit
Version 2.10.1208. Copyright (C) 2010 American Megatrends, Inc.

5.2 Advanced Settings



The following settings can be changed from this screen or one of its sub-menus:

Legacy OpROM Support

Launch PCE OpROM: Enable or disable the boot option for legacy network devices

Launch Storage OpROM: Enable or disable the boot option for legacy mass storage devices with option ROM

CPU Configuration

Set CPU configururations and display detected CPU information. The following settings can be changed.

Hyper-threading: Enable or disable the processor's hyper-threading feature
Enable for Windows XP and Linux, disable for other Oss

Limit CPUID Maximum: Enable or disable the Limit CPUID Maximum

Intel Virtualization Technology: Enable or disable virtualization
When enabled, a VMM can utilize the additional hardware capabilities

SATA Configuration

Select the operation mode of the SATA controller. The following setting can be changed.

SATA Controller(s): Enable or disable SATA devices

SATA Mode Selection: Set as Disable, IDE (default), AHCI or RAID

IDE sets the Serial ATA drives as Parallel ATA storage devices

AHCI allows the Serial ATA devices to use AHCI (Advanced Host Controller Interface)

RAID creates a RAID or Intel Matrix Storage configuration on Serial ATA devices

Intel Anti-Theft Technology Configuration

Configures the Intel Anti-Theft function. The following settings can be changed.

Intel Anti-Theft Technology: Enable or disable the Anti-Theft Technology function in the BIOS

Enter Intel AT Suspend Mode: Enable or disable a request that the platform enters AT suspend mode

USB Configuration

Sets the USB configurations. The following settings can be changed.

Legacy USB Support: Enable (default), disable or AUTO support for legacy USB

AUTO option disables legacy support if no USB devices are connected

EHCI Hand-off: Enable (default) or disable the EHCI hand-off feature

Do not disable the Hand-off option if you are running a Windows operating system with a USB device

Mass Storage Devices: This section displays device information when USB devices are detected

H/W Monitor 2

Displays PC Health Status including CPU temperature, system temperature, and system voltages.

Super I/O Configuration

Set up or configures the Super I/O functions for floppy disk controllers, parallel ports and serial ports. The following settings can be changed.

Floppy Disk Controller Sub-Menu

Floppy Disk Controller: Enable or disable the on-board floppy disk controller

Change Settings: Select the IO/IRQ of the device

Device Mode: Set to Read Write or Write Protect

Serial Port 1 Configuration Sub-Menu (identical to Serial Port 2 Configuration)

Serial Port: Enable or disable the serial port 1

Change Settings: Change serial port 1's port address and interrupt address

Device Mode: Set to Standard Serial Port Mode, IrDA 1.0 (HP SIR) Mode, or ASKIR Mode

Parallel Port Configuration Sub-Menu

Parallel Port: Enable or disable the parallel port (LPT/LPTE)

Change Settings: Change the parallel port's port address and interrupt address

Device Mode: Set to Standard Parallel Port Mode, EPP Mode, ECP Mode, or EPP Mode & ECP Mode

H/W Monitor

Displays PC Health Status including system temperature, fan speeds and system voltages of PBE-1700.

Sandybridge PPM Configuration

Configures the periodic permanent magnetic of the Sandybridge chip. The following settings can be changed.

EIST: Enable or disable the Intel SpeedStep feature

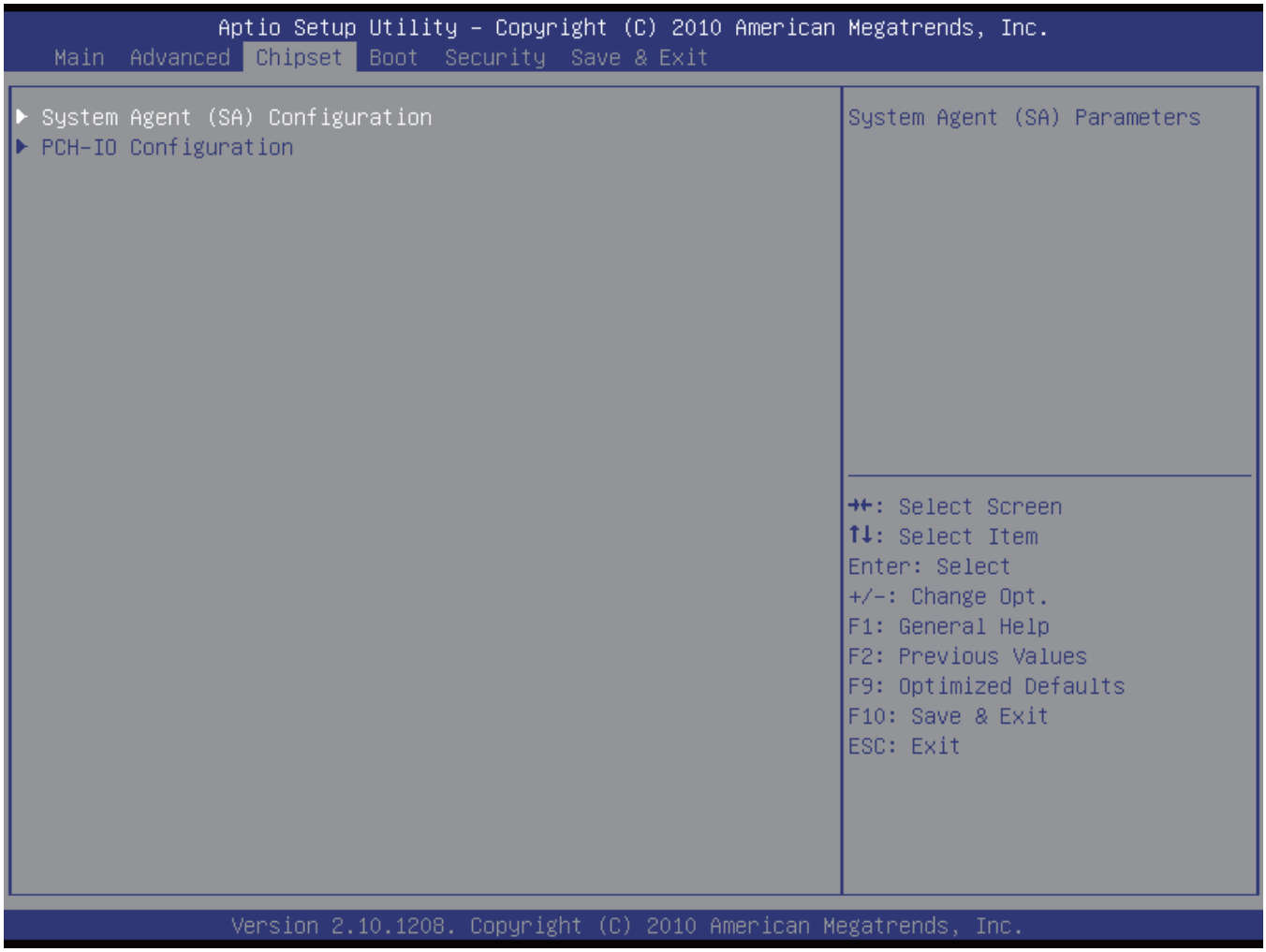
Turbo Mode: Enable or disable turbo mode

CPU C3 Report: Enable or disable the CPU C3 (ACPI C2) report to the OS

CPU C6 Report: Enable or disable the CPU C6 (ACPI C3) report to the OS

CPU C7 Report: Enable or disable the CPU C7 (ACPI C3) report to the OS

5.3 Chipset Settings


Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
System Agent (SA) Configuration
PCH-IO Configuration
System Agent (SA) Parameters
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit
ESC: Exit
Version 2.10.1208. Copyright (C) 2010 American Megatrends, Inc.

The following settings can be changed from this screen or one of its sub-menus:

System Agent (SA) Configuration

VT-d:	Enable or disable the SA CHAP device
Thermal Device:	Enable or disable the SA thermal device
Enable NB CRID:	Enable or disable the NB CRID workaround

Graphics Configuration Sub-Menu

Primary Display:	Set which graphics devices should be Primary Display or SG for switchable Gfx
Internal Graphics:	Enables IGD
GTT Size:	Select between 1MB and 2MB
Aperture Size:	Select between 128MB, 256MB and 512MB
DVMT Pre-Allocated:	Set the DVMT 5.0 fixed graphics memory size to between 0MB and 512MB
DVMT Total Gfx Mem:	Set the total graphics memory size to 128MB, 256MB or MAX
Gfx Low Power Mode:	Enable or disable low power mode, applicable for SFF only

LCD Control Sub-Menu

Primary IGFX Boot Display: Select the video device to be activated during POST
This has no effect if external graphics are present
A secondary boot display section will appear based on selection

LCD Panel Type: Select the LCD panel used by the internal graphics device

Panel Scaling: Set the LCD panel scaling as Auto, Off, or Force Scaling

Backlight Control: Set as PWM Inverted (default), PWM Normal, GMBus Inverted, or GMBus Normal

BIA: Select between VBIOS Default, Disabled, or Level 1/2/3/4/5

Spread Spectrum clock Chip: Set as Off (default), Hardware, or Software

Active LFP: Select between No LVDS, Int-LVDS, SDVO LVDS, and eDP Port-A

Panel Color Depth: Set the LFP panel color depth to 18-bit or 24-bit

DMI Configuration Sub-Menu

DMI Vc1/Vcp/Vcm Control: Enable or disable DMI Vc1/Vcp/Vcm

DMI Link ASPM Control: Set the state of the ASPM as L0s, L1, L0sL1, or Disabled

DMI Extended Synch Control: Enable or disable DMI extended synchronization

DMI Gen 2: Enable or diable DMI Gen 2

NB PCIe Configuration Sub-Menu

PEG0 – Gen X: Configure PEG0 to Auto, Gen1 or Gen2

PEG1 – Gen X: Configure PEG1 to Auto, Gen1 or Gen2

PEG2 – Gen X: Configure PEG2 to Auto, Gen1 or Gen2

PEG3 – Gen X: Configure PEG3 to Auto, Gen1 or Gen2

Always Enable PEG: Enable or disable the PEG slot

PEG ASPM: Set ASPM of the PEG device as Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1
This has no effect if PEG is not the currently active device

De-emphasis Control: Set the de-emphasis control on PEG to -6dB or -3.5dB

Memory Configuration Sub-Menu

DIMM profile: Set DIMM timing profile as Default DIMM profile, XMP profile 1, or XMP profile 2

Memory Frequency: Set maximum memory frequency as Auto, 1067, 1333, 1600, 1867, or 2133MHz

ECC Support: Enable or disable DDR ECC support

Max TOLUD: Set the maximum value of TOLUD
Dynamic adjusts TOLUD based on large MMIO length of installed graphics controller

NMode Support: Set NMode support as Auto, 1 N Mode, or 2 N Mode

Memory Scrambler: Enable or disable memory scrambler support

RMT Crosser Support: Enable of disable RmtCrosserEnable support

MRC Fast Boot: Enable or disable MRC fast boot

Force Cold Reset: Force cold reset or choose MRC cold reset mode
If ME 5.0MB is present, Force Cold Reset is required

Scrambler Seed Generation Off: Enable or disable generate scramble seed

Memory Remap: Enable or disable memory remap above 4G

Channel A DIMM Control: Enable or disable DIMMs in channel A

Memory Thermal Configuration Sub-Menu

Memory Thermal Management: Enable or disable memory thermal management

PECI Injected Temperature: Enable or disable memory temperatures injected to CPU via PECI

EXTT# via TS-on-Board: Enable or disable routing TS-on-Board's ALERT# and THERM# to EXTT# pins on PCH

EXTT# via TS-on-DIMM: Enable or disable routing TS-on-DIMM's ALERT# to EXTT# pins on PCH

Virtural Temperature Sensor (VTS): Enable or disable virtual temperature sensor

GT-Power Management Control Sub-Menu

RC6 (Render Standby): Enable or disabler render standby support

GT Overclocking Support: Enable or disable GT overclocking support

PCH-IO Configuration

PCIE Wake UP: Enable or disable PCIE Wake# to wake the system

Wake on RING: Enable or disable Wake on RING (WOR)

Azalia: Set Azalia control detection to Disabled, Enabled, or Auto

SLP_S4 Assertion Width: Select minimum assertion width of SLP_S4# signal

Restore AC Power Loss: Set the AC power state when power is reapplied after power failure

USB Configuration Sub-Menu

EHCI1 and EHCI2: Control the USB EHCI (USB 2.0) functions
One EHCI controller must always be enabled

USB Ports per-Port Disable Control: Enable or disable each of the USB ports (0~9)

PCI EXPRESS Configuration Sub-Menu

PCI Express Clock Gating: Enable or disable PCI Express clock gating for each root port

DMI Link ASPM Control: Controls the Active State Power Management on both NB side and SB side of the DMI Link

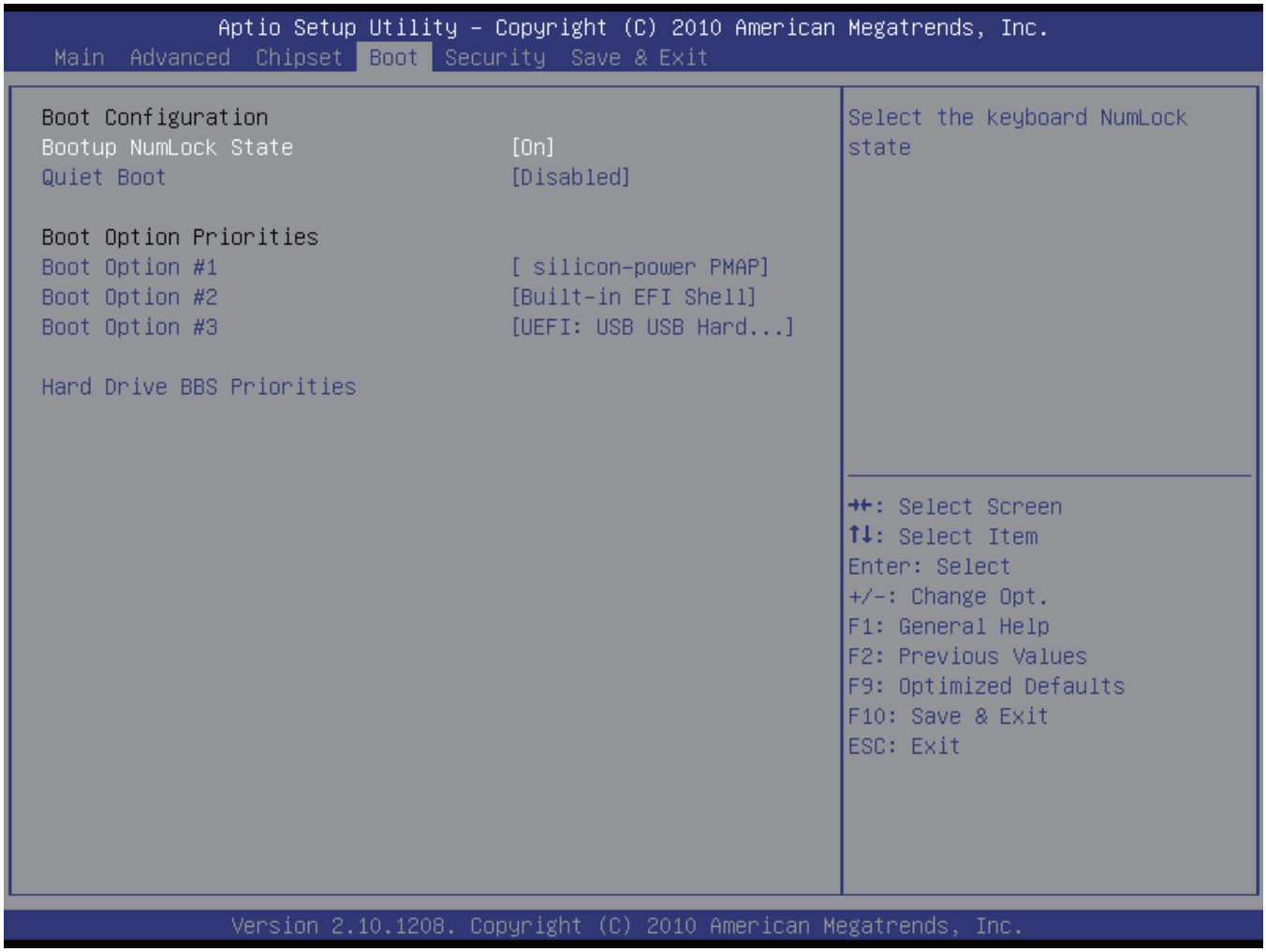
DMI Link Extended Synch Control: Enable or disable Extended Synch on SB side of the DMI Link

Subtractive Decode: Enable or disable Subtractive Decode

PCI Express Root Port X Sub-Menu (same for all ports 1-8)

Control the PCI Express Root Port for each port

5.4 Boot Settings


Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Boot Configuration
Bootup NumLock State [On]
Quiet Boot [Disabled]
Boot Option Priorities
Boot Option #1 [silicon-power PMAP]
Boot Option #2 [Built-in EFI Shell]
Boot Option #3 [UEFI: USB USB Hard...]
Hard Drive BBS Priorities
Select the keyboard NumLock state
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit
ESC: Exit
Version 2.10.1208. Copyright (C) 2010 American Megatrends, Inc.

Boot Configuration

Bootup NumLock State: Set On or Off whether the Num Lock key should be activated at boot up

Quiet Boot: Enable or disable the screen display when the system boots

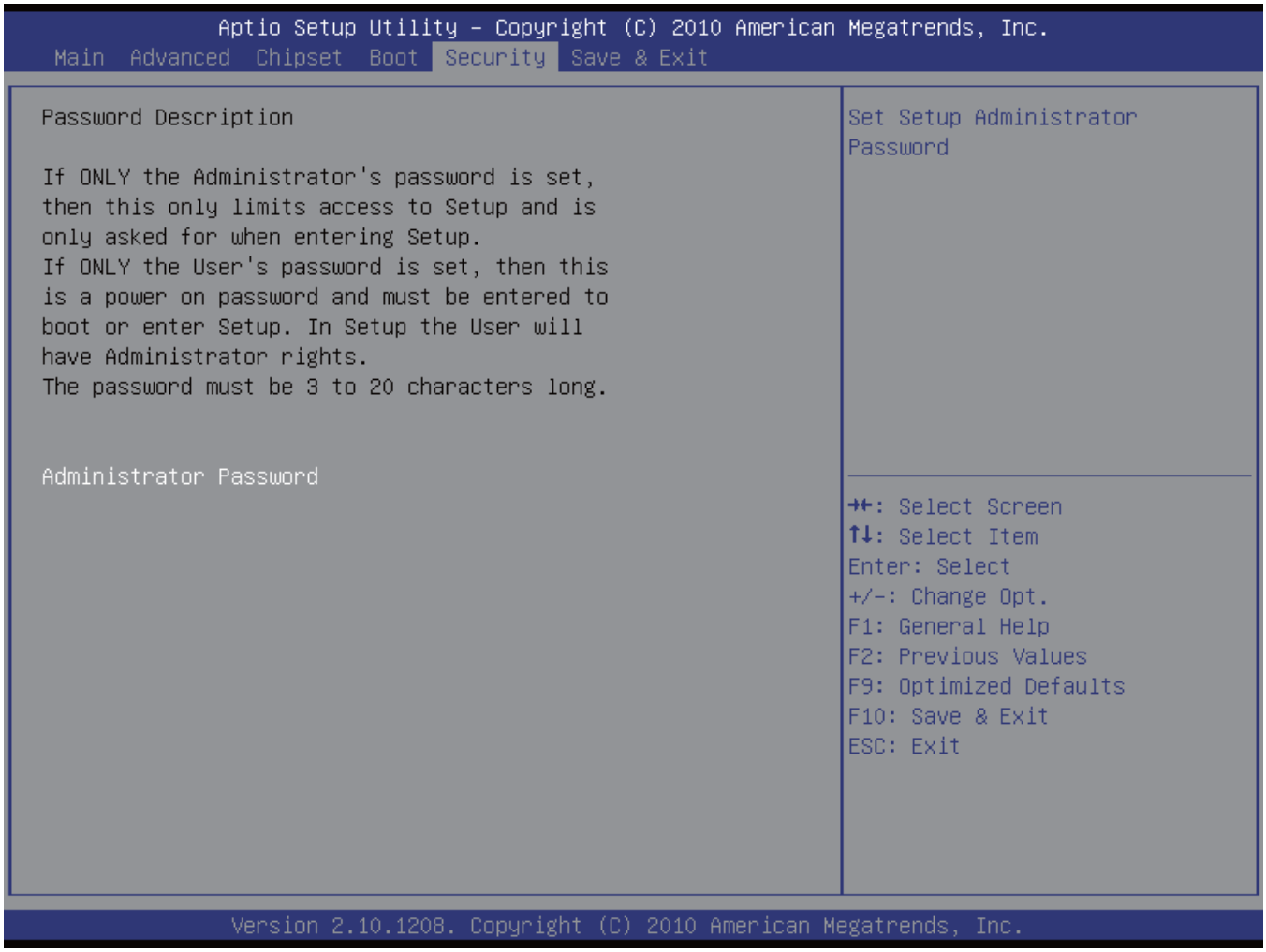
Boot Option Priorities

Select the boot sequence of the hard drives

Hard Drive BBS Priorities

Set the hard drive boot priority

5.5 Security Settings

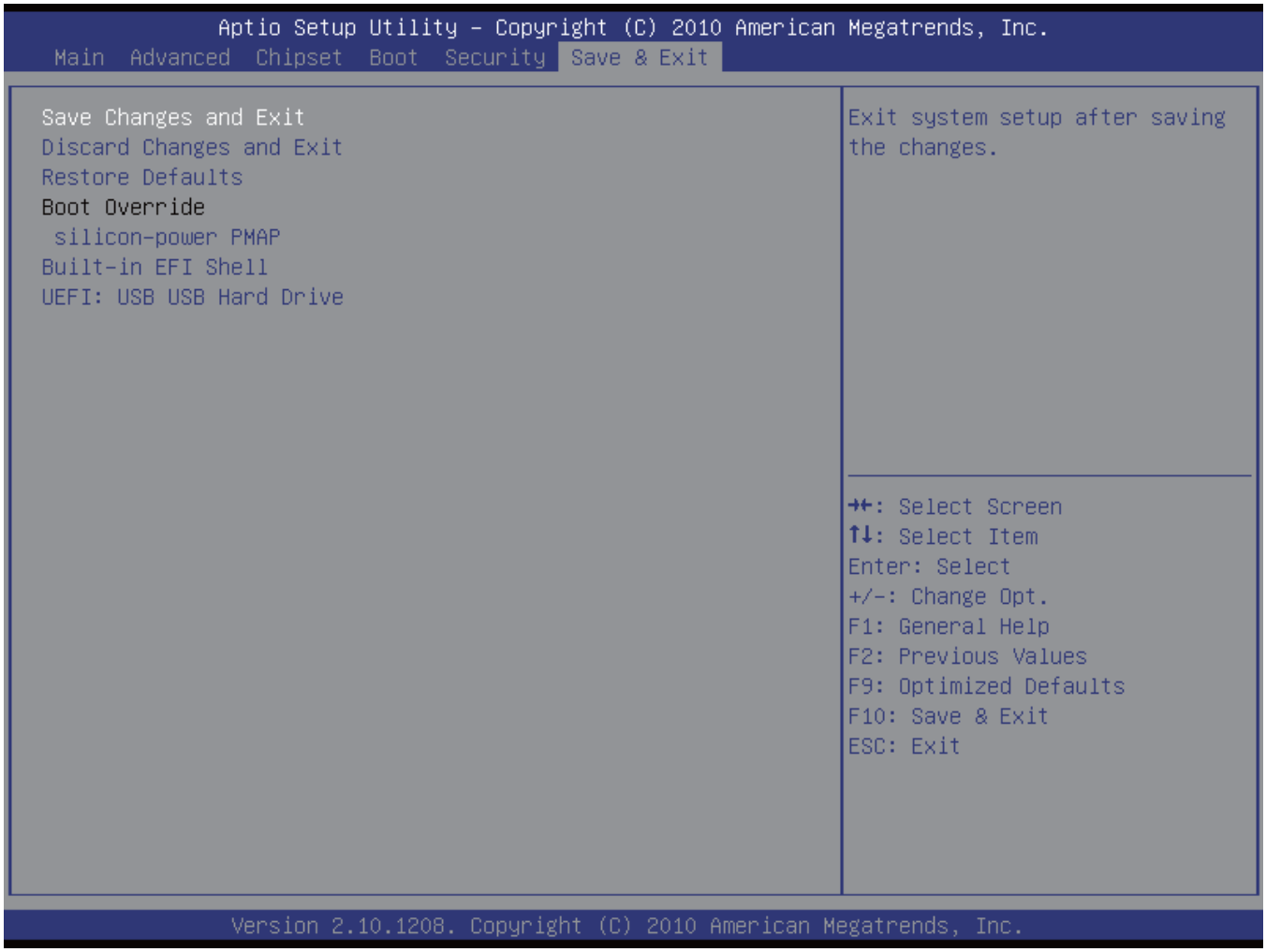

Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Password Description
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup.
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights.
The password must be 3 to 20 characters long.
Administrator Password
Set Setup Administrator Password
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit
ESC: Exit
Version 2.10.1208. Copyright (C) 2010 American Megatrends, Inc.

Administrator Password

Set or change an eight character administrator password

To disable a password, enter a blank password

5.6 Save & Exit Settings


Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Save Changes and Exit
Discard Changes and Exit
Restore Defaults
Boot Override
silicon-power PMAP
Built-in EFI Shell
UEFI: USB USB Hard Drive
Exit system setup after saving the changes.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit
ESC: Exit
Version 2.10.1208. Copyright (C) 2010 American Megatrends, Inc.

6. ANALOG I/O OPERATION

6.1 A/D Input Ranges and Resolution

The Vega baseboard uses a 16-bit A/D converter. This means that the analog input voltage can be measured to the precision of a 16-bit binary number. The maximum value of a 16-bit binary number is 2^{16} - 1, so the full range of numerical values that you can get from a Vega baseboard analog input channel is 0 - 65535.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of one in the A/D code, and is referred to as one Least Significant Bit (1 LSB).

6.2 Unipolar and Bipolar Inputs

The Vega baseboard can measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. The full-scale input voltage range depends on the Gain, Range, and Polarity bit settings in the Analog Configuration register (Base+11). In front of the A/D converter is a programmable gain amplifier that multiplies the input signal before it reaches the A/D. This gain circuit has the effect of scaling the input voltage range to match the A/D converter for better resolution. In general, you should select the highest gain possible that will allow the A/D converter to read the full range of voltages over which your input signals varies. If the gain is too high, the A/D converter clips at either the high end or low end, and you will be unable to read the full range of voltages on your input signals.

6.3 Ranges and Resolutions

The table below lists the full-scale input range for each valid analog input configuration. The parameters Polarity, Range and Gain are combined to create the value "Code", which is written to the Analog Configuration register (Base+11) to get the input range shown. A total of nine different input ranges are possible. The range programming codes 4, 5, 6, and 7 are invalid and that range codes 9–11 are equivalent to range codes 0–2.

Polarity	*Range*	*Gain*	*Code*	*Input Range*	*Resolution (1 LSB)*
Bipolar	5V	1	0	± 5V	153µV
Bipolar	5V	2	1	± 2.5V	76µV
Bipolar	5V	4	2	± 1.25V	38µV
Unipolar	5V	1	4		Invalid Setting
Unipolar	5V	2	5		Invalid Setting
Unipolar	5V	4	6		Invalid Setting
Unipolar	5V	8	7		Invalid Setting
Bipolar	10V	1	8	± 10V	305µV
Bipolar	10V	2	9	± 5V	153µV
Bipolar	10V	4	10	± 2.5V	76µV
Bipolar	10V	8	11	± 1.25V	38µV
Unipolar	10V	1	12	0-10V	153µV
Unipolar	10V	2	13	0-5V	76µV
Unipolar	10V	4	14	0-2.5V	38µV

6.3.1 Conversion Formulas

The 16-bit value returned by the A/D converter is always a two's complement number ranging from -32768 to 32767, regardless of the input range. This is because the input range of the A/D is fixed at ±10V. The input signal is actually magnified and shifted to match this range before it reaches the A/D. For example, for an input range of 0–10V, the signal is first shifted down by 5V to ±5V and then amplified by two to become ±10V. Therefore, two different formulas are needed to convert the A/D value back to a voltage, one for bipolar ranges, and one for unipolar ranges.

To convert the A/D value to the corresponding input voltage, use the following formulas, depending on bipolar or unipolar mode of operation.

6.3.1.1 Conversion Formula for Bipolar Input Ranges

Input voltage = A/D code / 32768 * Full-scale input range

Example:

Given, Input range is ± 5V and A/D code is 17761.

Therefore,

Input voltage = 17761 / 32768 * 5V = 2.710V.

For a bipolar input range,

1 LSB = 1/32768 * Full-scale voltage.

The following table shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage):

A/D Code	***Input Voltage Symbolic Formula***	***Input Voltage for ±5V Range***
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	V_{FS} - 1 LSB	4.9998V

6.3.1.2 Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D code + 32768) / 65536 * Full-scale input range

Example:

Given, Input range is 0–10V and A/D code is 17761.

Therefore,

Input voltage = (17761 + 32768) / 65536 * 10V = 7.7103V.

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

The table on the following illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

A/D Code	*Input Voltage Symbolic Formula*	*Input Voltage for 0-5V Range*
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.153 mV
...	...	...
-1	V_{FS} / 2 - 1 LSB	4.99985V
0	V_{FS} / 2	5.0000V
1	V_{FS} / 2 + 1 LSB	5.00015V
...	...	...
32767	V_{FS} - 1 LSB	9.9998V

6.4 A/D Control Signals

This section documents the signals used to control the A/D circuit. This circuit consists of several muxes, a PGA, a range/polarity phase, a serial A/D converter, a FIFO internal to the FPGA, and several sources of A/D trigger.

There is always a “current A/D channel”, represented by ADCH<3:0> @ base+7 (read only). This is the channel that will be sampled next by the A/D converter. The outputs PADCH<2:0> (ADCH<2:0> on the board) represent the MUX channel to be sampled, together with MUXENx will determine which of the 16 AD channels will be sampled:

ADCH<3:0> = <MUXEN1/0, PADCH2, PADCH1, PADCH0> any of 16 channels in Single Ended mode. MUXEN1/0 is high when the mux enable outputs are MUXEN[1:0]=10b (i.e. channels 15 to 8 are selected). It is low when MUXEN[1:0]=01b (i.e. channels 7 to 0 are selected).

ADCH<3:0> = < 0, PADCH2, PADCH1, PADCH0> any of 8 channels in Differential mode.

The PADCH<2:0> outputs along with the CALPOL output (set in Page 1, Base +14) control the VCAL value as shown in the following table (where SW is the input port of the analog mux):

CALPOL	PADC<2:0>	SW	VCAL
0	000	S1	12.21 to 12.50mV
0	001	S2	1.244 to 1.251V
0	010	S3	2.478 to 2.488V
0	011	S4	4.954 to 4.96V
1	000	S1	-12.21 to -12.50mV
1	001	S2	-1.244 to -1.251V
1	010	S3	-2.478 to -2.488V
1	011	S4	-4.954 to -4.96V
X	100	S5	AGND
X	101	S6	15V / 10 ~ 1.5V
X	110	S7	VIN /10 ~ .7 ot 3.2V
X	111	S8	DAC Temp Sensor

CALPOL = 0 is the initial value in order to be compatible with previous software.

Whenever base + 2 is written, ADCH3-0 is set to L3-0. ADCH3-0 increments on each ADR/C pulse, except that if ADCH3-0 = H3-0, then on the next ADR/C pulse ADCH3-0 is set to L3-0. It is valid for ADCH3-0 to wrap around past 15 to 0 and continue to increment. Thus a configuration of L3-0 = 14 and H3-0 = 1 is valid. In this case, ADCH3-0 will cycle through the values 14, 15, 0, 1, 14, 15, 0, 1, …

The MUXEN[1:0] output signals control which mux feeds inputs to the PGA. If L3 is set to 1, MUXEN[1:0] is set to 10b. If it is set to 0, then MUXEN[1:0] is set to 01b. If the CALMUX bit in page 1 is set (‘1’), CALEN goes high and all other MUXENx bits go low (i.e. there is no output from either mux). Otherwise CALEN is low.

ADDATACLK is the AD serial data clock up to 28.5MHz. FPGA will drive ADDATACLK at the rate of the input clock 24MHz.

ADDATA is the serial data output. Data is synchronized with ADDATACLK. Data format is binary 2’s complement.

ADR/C is the Read/Convert input. A falling edge on ADR/C starts a conversion while a raising edge starts the transmission of data from the previous conversion.

ADR/C is default high and pulses low for 1 system clock for each A/D conversion to be generated when activated (hereafter called the A/D command). The A/D command is as follows: If SCANEN=0, ADR/C will pulse low one time for the current A/D channel. If SCANEN=1, ADR/C will pulse low one time for each channel in the scan range L3-0 to H3-0 in base + 2. The interval between pulses is defined by SCANINT in page 2 base + 14.

If AINTE=0, then if ADCLK=0, the A/D command occurs on a write to base+0, and if ADCLK=1, the A/D command occurs on a falling edge of EXTTRIG.

If AINTE=1, then if ADCLK=0, the A/D command occurrs on a falling edge of the outout from Counter 0, and if ADCLK=1, the A/D command occurs on a falling edge of EXTTRIG.

ADBUSY is an input connected the BUSY output from the ADC. The BUSY output falls when a conversion is started and remains low until the conversion is completed and the data is latched into the output shift register.

ADG<1:0> determine the gain of the PGA and are based on the ADG<1:0> bits at base +3.

ADG<1:0> = 00 = x1

ADG<1:0> = 01 = x2

ADG<1:0> = 10 = x4

ADG<1:0> = 11 = x8

SE/DIFF is an output. 0 for Single Ended AD sampling, 1 for Differential AD sampling. Controlled by SE/DIFF at base+3.

ADUNIP output to CMOS switch. Logic 1 sets the AD in unipolar mode. Logic 0 sets the AD in bipolar mode.

CALEN is an output. 0 by default and in normal AD sampling mode, 1 when CALMUX is enabled.

<SE/DIFF, CALEN> = 1 feeds the AD with VCAL.

<SE/DIFF, CALEN> = 2 feeds the AD with VOUT0. Output of the channel 0 on the DAC.

The FIFO should use the internal RAM of the FPGA. The initial design will use 4KB of RAM, or 2K samples (each sample is 16 bits). The new internal controller should emulate the EF, HF, FF and OVF signals. (FF) FIFO_FULL#, (HF) FIFO_HF# and (EF) FIFO_EMPTY# are outputs that reflect the state of the internal FIFO. They serve no functional purpose other than debug. Their values are also reflected in the corresponding read-back bits at base+6.

6.5 A/D Sampling Methods

6.5.1 Sampling Modes

There are several different A/D sampling modes available on a Vega baseboard. The desired mode is selected with the FIFOEN and SCANEN bits at the FIFO Control register (Base+7), and the ADINTE bit in the Interrupt Control register (Base+9).

> ***Note:*** *If interrupts are not enabled, the FIFO should not be enabled. FIFO storage is only useful when interrupts are used. Otherwise, the FIFO has no effect.*

All of these features may be selected as arguments to function calls in the driver software. The control register details are provided for completeness and for programmers not using the driver.

SCANEN	*FIFOEN*	*ADINTE*	*Mode*	*Description*
No	No	No	Single Conversions	The most basic sampling method. Used for low-speed sampling (typically up to about 100 Hz) under software control where a precise rate is not required, or under external control where the rate is slow. Consists of either one channel or multiple channels sampled one at a time.
Yes	No	No	Scan Conversions	Used to sample a group of consecutively numbered channels in rapid succession, under software or external control. The time between samples in a scan is programmable between 5 to 20 microseconds, while the time between scans depends on the software or external trigger and may be very short or very long, but is usually less than about 100 Hz (above this rate use interrupt scans below).

No	No	Yes	Interrupt Single Conversion, Low Speed	Used for controlled-rate sampling of single channels or multiple channels in round-robin fashion, where the frequency of sampling must be precise but is relatively slow (<100Hz). The sampling clock comes from the on-board counter/timer or from an external signal. The interval between all A/D samples is identical.
Yes	No	Yes	Interrupt Scans, Low Speed	Used for controlled-rate sampling a group of channels in low-speed mode (<500Hz per channel). Each sampling event consists of a group of channels sampled in rapid succession. The time between scans is determined by the sample rate.
No	Yes	Yes	Interrupt Single Conversions, High Speed	Intended for medium- to high-speed operation (recommended above about 500 Hz). Can support sampling rates up to the board's maximum of 250,000 Hz. May also be used at slower rates if desired. The sampling clock comes from the on-board counter/timer or from an external signal.
Yes	Yes	Yes	Interrupt Scan Conversions	Used for high-speed sampling of a group of channels where the scan rate is high. The sampling clock comes from the on-board counter/timer or from an external signal.

6.5.2 FIFO Description

The Vega baseboard uses a 2048-sample FIFO (First In First Out) memory buffer to manage A/D conversion data. The FIFO is used to store A/D data between the time it is generated by the A/D converter and the time it is read by the user program. In enhanced mode, the entire 2048-sample FIFO is available. In normal mode only 1024 samples are available. The FIFO may be enabled and disabled under software control.

In single-conversion mode, the FIFO features are not generally needed so FIFO use should not be selected (although the FIFO is actually being used). Each A/D sample is stored in the FIFO. When the software reads the data, it reads it out of the FIFO. In low-speed sampling, each time a conversion occurs, the program reads the data, so there is always a one-to-one correspondence between sampling and reading. Thus, the FIFO contents never exceed one sample.

For high-speed sampling or interrupt operation, the FIFO significantly reduces the amount of software overhead in responding to A/D conversions. Using the FIFO also reduces the interrupt rate on the bus because it enables the program to read multiple samples at a time. In addition, the FIFO is required for sampling rates in excess of the maximum interrupt rate possible on the bus. Generally, the fastest sustainable interrupt rate on the ISA bus running DOS is around 40,000 per second. Since the Vega baseboard can sample up to 250,000 times per second, the FIFO is needed to reduce the interrupt rate at high speeds. When the interrupt routine runs, it reads multiple samples from the FIFO. The interrupt rate is equal to the sample rate divided by the number of samples read each interrupt. On Vega, this number is programmable using the FIFO Threshold register (Base+6). The usual value is 1/2 the maximum FIFO depth, or 1024 samples. Therefore, the maximum interrupt rate for Vega is reduced to 996 per second, which is easily sustainable on any popular operating system.

> ***Note:*** *If both scan and FIFO operations are enabled, the interrupt occurs at the programmed FIFO threshold and the interrupt routine reads the indicated number or samples and then exits. This happens even if the number of samples is not an integral number of scans. For example, if you have a scan size of 10 and a FIFO threshold of 256, the first time the interrupt routine runs, it reads 256 samples, consisting of 25 full scans of all 10 channels followed by 6 samples from the next scan. The next time the interrupt routine runs, it reads the next 256 samples, consisting of the remaining 4 samples from the last scan it started to read, the next 25 full scans of 10 samples, and the first 2 samples of the next scan. (If you are using the Universal Driver software, this continues until the interrupt routine ends in either one-shot or recycle mode. In one-shot mode, the last time the interrupt routine runs it reads the entire contents of the FIFO, making all data available.)*

6.5.3 Scan Sampling

A scan is defined as a quick burst of samples of multiple consecutive channels. For example, you may want to sample channels 0–15 at one time, and repeat the operation each second, resulting in a scan at a frequency of 1 Hz. Each time the A/D clock occurs (software command, timer, or external trigger), all 16 channels are sampled in high-speed succession. There is a short delay of 4–20 microseconds between each sample in the scan. Since each clock pulse causes all channels to be sampled, the effective sampling rate for each channel is the same as the programmed rate, and the total sampling rate is the programmed sampling rate times the number of channels in the scan range.

Scan sampling is independent of FIFO operation, and can be enabled independently.

6.5.4 Sequential Sampling

In sequential sampling, each clock pulse results in a single A/D conversion on the current channel. If the channel range is set to a single channel (high channel = low channel), each conversion is performed on the same input channel. If the channel range is set to more than one channel (high channel > low channel), then the channel counter increments to the next channel in the range, and the next conversion is performed on that channel. When a conversion is performed on the high channel, the channel counter resets to the low channel for the next conversion. The intervals between all samples are equal. Since each clock pulse results in only one channel being sampled, the effective sampling rate is the programmed sampling rate divided by the number of channels in the channel range.

6.6 A/D Conversion

This section describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (without the driver software).

All A/D conversions are stored in an on-board FIFO (first in first out memory). The FIFO can hold up to 2048 samples. Each time an A/D conversion is finished, the data is stored in the FIFO and the FIFO counter increments by 1. Each time you read A/D data, you are actually reading it out of the FIFO and the FIFO counter decrements by 1. When the FIFO is empty, the data read from it is undefined; you may continue to read the last sample, or you may read all 1s.

You can either read each A/D sample when they become available, or you can wait for a collection of samples (up to 2048 maximum) and read all of the samples at once.

To be sure that you are getting only current A/D data, always reset the FIFO before you start an A/D operation. This prevents errors caused by leaving data in the FIFO from a previous operation. To reset the FIFO, write a 1 to the FIFORST bit of the FIFO Control register (Base+7). This bit is not a real register bit, but it triggers a command in the board's controller chip; therefore, you do not need to write a 1 followed by a 0.

```
outp(Base+7, 0x02); // resets the FIFO and clears SCANEN and FIFOEN
outp(Base+7, 0x0A); // resets the FIFO and SCANEN but leaves FIFOEN set
```

Note: *writing to the FIFORST bit also affects the values of other bits in this register.*

This register also contains a FIFO enable bit, FIFOEN, which only has meaning during A/D interrupt operations. The FIFO is always enabled and is always in use during A/D conversions.

Perform an A/D conversion according to the following steps:

- Select the input channel
- Select the input range
- Wait for analog input circuit to settle
- Initiate an A/D conversion
- Wait for the conversion to finish
- Read the data from the board
- Convert the numerical data to a meaningful value

Each of these steps is discussed in detail on the following pages.

The control registers associated with A/D conversions are provided below for reference.

Base +	R/W	7	6	5	4	3	2	1	0
0	W	STARTAD							
0	R	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	R	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	R/W	-	-	-	L4	L3	L2	L1	L0
3	R/W	-	-	-	H4	H3	H2	H1	H0
8	R	**STS**	S/D1	S/D0	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
11	W	**-**	-	SCINT1	SCINT0	RANGE	ADBU	G1	G0
11	R	WAIT	RSVD	SCINT1	SCINT0	RANGE	ADBU	G1	G0

STARTAD	Writing any value to this register will trigger an AD conversion
AD15-0	A/D data value
L3-L0	Low channel of selected A/D range (0–31)
H3-H0	High channel of selection A/D range (0–31)
STS	AD conversion status bit. 0 = A/D is idle, 1 = A/D is busy, must wait for completion.
WAIT	A/D circuit settling indicator. 0 = circuit is idle, 1 = A/D is busy.

If you are going to sample the same channel multiple times or sample multiple consecutive channels with the same input range, you only need to perform steps 1–3 once, and then you can repeat steps 4-6 or 4-7 as many times as desired.

6.6.1 Select the Input Channel

The Vega baseboard contains a channel counter circuit that controls which channel is sampled on each A/D conversion command. The circuit uses two channel numbers called the low channel and high channel. These are stored in the A/D Low Channel and A/D High Channel registers (Base+2 and Base+3). The circuit starts at the low channel and automatically increments after each A/D conversion until the high channel is reached. When an A/D conversion is performed on the high channel, the circuit resets to the low channel and starts over again. This behavior enables you simplify your software by setting the channel range just once.

To read continuously from a single channel, write the same channel number to both the low channel and high channel registers.

To read from a series of consecutively numbered channels, write the starting channel to the A/D Low Channel register (Base+2) and the ending channel to the A/D High Channel register (Base+3).

To read from a group of non-consecutive channels, you must treat each as a single channel, as described above.

For example: To select channels 0–31 for the operation…

```
outp(base+2, 0x00) ;
outp(base+3, 0x1F) ;
```

6.6.2 Select the Input Range

Select the code corresponding to the desired input range and write it to the RANGE bit of the Analog Configuration register (Base+11). You only need to write to this register if you want to select a different input range from the one used for the previous conversion. If all channels are using the same input range, you can configure this register just once at the beginning of your procedure.

You can read the current value of this register by reading from the analog Configuration register (Base+11).

```
outp(base+11, 0x00) ; // 5V, BIPOLAR, GAIN = 1
outp(base+11, 0x0E) ; // 10V, UNIPOLAR, GAIN = 4
```

6.6.3 Wait for Analog Input Circuit to Settle

After changing either the input channel or the input range, you must allow the circuit to settle on the new value before performing an A/D conversion. The settling time is long compared to software execution times, so a timer is provided on board to indicate when it is safe to proceed with A/D sampling. The WAIT bit in the Analog I/O Read-back register (Base+11) indicates when the circuit is settling and when it is safe to sample the input. When WAIT is 1, the board is settling. When WAIT is 0, the board is ready for an A/D conversion.

```
while ( inp ( base+11) & 0x80 ); // wait for AD to be available
```

6.6.4 Perform an A/D Conversion on the Current Channel

To start an A/D conversion, simply write to the A/D Start Conversion register (Base+0). Any value may be written to the register.

```
outp(base, 0xFF) ; // trigger an AD conversion
```

6.6.5 Wait for the Conversion to Finish

The A/D converter takes about four microseconds to complete a conversion. If you try to read the A/D converter data immediately after starting a conversion, you will read invalid data. Therefore, the A/D converter provides a status signal to indicate whether it is busy or idle. This signal can be read back as the STS bit in the A/D Status register (Base+8). When the A/D converter is busy (performing an A/D conversion) the STS bit is 1. When the A/D converter is idle (conversion is done and data is available) the STS bit is 0.

```
while ( inp ( base + 8 ) & 0x80 ); // wait for AD conversion to end
```

6.6.6 Read the Data from the Board

Once the conversion is complete, you can read the data back from the A/D converter. The data is 16 bits wide and is read back in two 8-bit bytes from the A/D LSB and A/D MSB registers (Base+0 and Base+1). The low byte, A/D LSB register, must be read first.

Note: *Reading data from an empty FIFO returns unpredictable results.*

The following pseudo-code illustrates how to read and construct the 16-bit A/D value with 8-bit accesses:

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

Alternatively, the value can be read as one 16-bit value, which is preferred since this method increases overall system bandwidth while reading data from the FIFO. For example:

```
Data = inpw(base); // Where the MSB and LSB are read in one access
```

The final data ranges from 0 to 65535 (0 to 256 - 1) as an unsigned integer. This value must be interpreted as a signed integer ranging from -32768 to +32767.

As noted above, all A/D conversions are stored in an on-board FIFO, which can hold up to 1024 samples in enhanced mode or 512 samples in normal mode. Whenever you read A/D data you are actually reading it out of the FIFO. Therefore, you can read each A/D sample as soon as it is ready, or you can wait until you take a collection of samples (up to 1024 maximum) and then read them all out in sequence.

6.6.7 Convert the numerical data to a meaningful value

The conversion formulas, above, describe how to convert the data back to the original input voltage. You may also convert the result into engineering units. The two conversions can be done sequentially, or the formulas can be combined into a single formula.

6.6.8 A/D Conversion Using Interrupts

Vega can generate hardware interrupts to manage A/D conversions. Interrupt-based A/D conversions are used in several situations.

- High-speed sampling.
- Applications that need a precise sampling rate.
- Applications that base the sampling rate on an external clock.

The Universal Driver functions *dscADSampleInt()* and *dscADSetSettings()* manage all of the required parameters to generate interrupt-based A/D conversions. Below is a checklist to help you configure the function call properly. All parameters are passed in the data structure of type *DSCAIOINT* for function *dscADSampleInt()* except for the input range.

A/D channel range (low channel, high channel).

On Vega, the channel numbers range from 0 to 31. Some channel numbers may not be available, depending on the single-ended/differential configuration mode as explained on page 11. During interrupt-based A/D conversions, the channels being sampled must be consecutive in number. To sample only a single channel, set the low channel and high channel to the same channel number. To sample a range of channels, set the low and high channels accordingly.

Input voltage range.

During interrupt-based A/D conversions, the input voltage range must be the same for all channels. Select the input range from the list of codes found in the Analog Input Ranges and Resolution section of this document. This parameter is set with the function *dscADSetSettings()* prior to calling *dscADSampleInt()*.

A/D Clock source, internal or external.

For internal clocking, the on-board 32-bit counter/timer is programmed to the desired sample rate. For external clocking, the signal EXTCLK/IN3 on connector J31, pin 31, controls sampling. Falling edges on this pin generate A/D conversions. The signal is edge sensitive; holding it low generates one conversion.

A/D conversion rate, if using internal clock.

If internal clocking is selected, provide the desired sample rate in Hz as a floating value. The maximum sample rate is 250,000 per second (maximum A/D operating speed), and the slowest rate is .000024383 Hz (100 KHz input / 232), or approximately 1 sample every 42,950 seconds (approximately 11.9 hours).

External gating enable.

You may choose to allow an external signal, EXTGATE, on connector J31, pin 32, to control the sampling. When the signal is high, sampling occurs, and when it is low, sampling pauses. External gating works with both internal and external clocking. This pin is connected to a 4.7K pull-up resistor.

One-shot vs. recycle mode (when using the Universal Driver APIs).

In one-shot mode, the operation occurs one time and then stops, and the parameter *num_*conversions determines the number of samples taken. In recycle mode, the operation runs repeatedly until you stop the operation by calling *dscCancelOp()*. In this case, the parameter *num_*conversions indicates the size of the memory buffer or array used to store the samples. Once the buffer is filled, the data is stored starting at the beginning again, causing the old data to be overwritten. In this situation, you only have access to the latest number of samples equal to *num_*conversions, and you must read the data out of the buffer before it is overwritten. The function *dscGetStatus()* can be used to indicate the current buffer position, which is the location at which the next data value will be stored.

6.7 D/A Conversion

This section documents the signals used to control the A/D circuit. This circuit consists of several muxes, a PGA, a range/polarity phase, a serial A/D converter, a FIFO internal to the FPGA, and several sources of A/D trigger.

There is always a "current A/D channel", represented by ADCH<3:0> @ base+7 (read only). This is the channel that will be sampled next by the A/D converter. The outputs PADCH<2:0> (ADCH<2:0> on the board) represent the MUX channel to be sampled, together with MUXENx will determine which of the 16 AD channels will be sampled:

ADCH<3:0> = <MUXEN1/0, PADCH2, PADCH1, PADCH0> any of 16 channels in Single Ended mode. MUXEN1/0 is high when the mux enable outputs are MUXEN[1:0]=10b (i.e. channels 15 to 8 are selected). It is low when MUXEN[1:0]=01b (i.e. channels 7 to 0 are selected).

ADCH<3:0> = < 0, PADCH2, PADCH1, PADCH0> any of 8 channels in Differential mode.

The PADCH<2:0> outputs along with the CALPOL output (set in Page 1, Base +14) control the VCAL value as shown in the following table (where SW is the input port of the analog mux):

CALPOL	PADC<2:0>	SW	VCAL
0	000	S1	12.21 to 12.50mV
0	001	S2	1.244 to 1.251V
0	010	S3	2.478 to 2.488V
0	011	S4	4.954 to 4.96V
1	000	S1	-12.21 to -12.50mV
1	001	S2	-1.244 to -1.251V
1	010	S3	-2.478 to -2.488V
1	011	S4	-4.954 to -4.96V
X	100	S5	AGND
X	101	S6	15V / 10 ~ 1.5V
X	110	S7	VIN /10 ~ .7 ot 3.2V
X	111	S8	DAC Temp Sensor

CALPOL = 0 is the initial value in order to be compatible with previous software.

Whenever base + 2 is written, ADCH3-0 is set to L3-0. ADCH3-0 increments on each ADR/C pulse, except that if ADCH3-0 = H3-0, then on the next ADR/C pulse ADCH3-0 is set to L3-0. It is valid for ADCH3-0 to wrap around past 15 to 0 and continue to increment. Thus a configuration of L3-0 = 14 and H3-0 = 1 is valid. In this case, ADCH3-0 will cycle through the values 14, 15, 0, 1, 14, 15, 0, 1, …

The MUXEN[1:0] output signals control which mux feeds inputs to the PGA. If L3 is set to 1, MUXEN[1:0] is set to 10b. If it is set to 0, then MUXEN[1:0] is set to 01b. If the CALMUX bit in page 1 is set ('1'), CALEN goes high and all other MUXENx bits go low (i.e. there is no output from either mux). Otherwise CALEN is low.

ADDATACLK is the AD serial data clock up to 28.5MHz. FPGA will drive ADDATACLK at the rate of the input clock 24MHz.

ADDATA is the serial data output. Data is synchronized with ADDATACLK. Data format is binary 2's complement.

ADR/C is the Read/Convert input. A falling edge on ADR/C starts a conversion while a raising edge starts the transmission of data from the previous conversion.

ADR/C is default high and pulses low for 1 system clock for each A/D conversion to be generated when activated (hereafter called the A/D command). The A/D command is as follows: If SCANEN=0, ADR/C will pulse low one time for the current A/D channel. If SCANEN=1, ADR/C will pulse low one time for each channel in the scan range L3-0 to H3-0 in base + 2. The interval between pulses is defined by SCANINT in page 2 base + 14.

If AINTE=0, then if ADCLK=0, the A/D command occurs on a write to base+0, and if ADCLK=1, the A/D command occurs on a falling edge of EXTTRIG.

If AINTE=1, then if ADCLK=0, the A/D command occurrs on a falling edge of the outout from Counter 0, and if ADCLK=1, the A/D command occurs on a falling edge of EXTTRIG.

ADBUSY is an input connected the BUSY output from the ADC. The BUSY output falls when a conversion is started and remains low until the conversion is completed and the data is latched into the output shift register.

ADG<1:0> determine the gain of the PGA and are based on the ADG<1:0> bits at base +3.

ADG<1:0> = 00 = x1

ADG<1:0> = 01 = x2

ADG<1:0> = 10 = x4

ADG<1:0> = 11 = x8

SE/DIFF is an output. 0 for Single Ended AD sampling, 1 for Differential AD sampling. Controlled by SE/DIFF at base+3.

ADUNIP output to CMOS switch. Logic 1 sets the AD in unipolar mode. Logic 0 sets the AD in bipolar mode.

CALEN is an output. 0 by default and in normal AD sampling mode, 1 when CALMUX is enabled.

<SE/DIFF, CALEN> = 1 feeds the AD with VCAL.

<SE/DIFF, CALEN> = 2 feeds the AD with VOUT0. Output of the channel 0 on the DAC.

The FIFO should use the internal RAM of the FPGA. The initial design will use 4KB of RAM, or 2K samples (each sample is 16 bits). The new internal controller should emulate the EF, HF, FF and OVF signals. (FF) FIFO_FULL#, (HF) FIFO_HF# and (EF) FIFO_EMPTY# are outputs that reflect the state of the internal FIFO. They serve no functional purpose other than debug. Their values are also reflected in the corresponding read-back bits at base+6.

Please refer to Diamond Systems' Universal Driver 7.0 User Manual for information on using and programming the analog I/O.

7. PULSE WIDTH MODULATORS

Vega offers four 24-bit pulse width modulator (PWM) circuits. The PWMs are programmed using a 24-bit PWM data register PWMD23-0 and an 8-bit command register PWCMD3-0 + PWM2-0 + PWMCD.

Each PWM consists of a pair of 24-bit down counters named C0 and C1. The C1 counter defines the duty cycle (active portion of the signal), and the C0 counter defines the period of the signal. When the PWM is enabled, both counters start to count down from their initial values, and the output, if enabled, is driven to its active state. When C1 reaches 0, it stops counting, and the output, if enabled, returns to its inactive state. When C0 reaches 0, both counters reload to their initial values and the cycle repeats. If C1 = 0 then duty cycle = 0. If C1 = C0, then duty cycle = 100% (the output should be glitch free).

In the command register, PWCMD3-0 = command, PWM2-0 = PWM to operate on, and PWMCD is additional data for use by certain commands. The default settings for all parameters is 0 since the default / reset value for all registers in this circuit is 0.

PWM commands are as follows (PWCMD3-0):

0000 Stop all / selected PWM as indicated by PWMCD.

0 = stop all PWMs (opposite polarity for “all” compared to other commands)

1 = stop PWM selected with PWM2-0

Command 0x00 = stop all PWMs.

0001 Load counter C0 or C1 selected by PWMCD:

0 = load C0 / period counter

1 = load C1 = duty cycle counter

0010 Set polarity for output according to PWMCD. The pulse occurs at the start of the period.

0 = pulse high

1 = pulse low

0011 Enable/disable pulse output as indicated by PWMCD

0 = disable pulse output; output = opposite of polarity setting from command 0010

1 = enable pulse output

0100 Clear all / selected PWM as indicated by PWMCD

0 = clear PWM selected with PWM2-0

1 = clear all PWMs

0101 Enable/disable PWM outputs on DIO port D according to PWMCD

0 = disable output

1 = enable output on P_DIODn where n = PWM number + 2; this forces P_DIODn to output mode

0110 Select clock source for PWM indicated by PWM2-0 according to PWMCD (both counters C0 and C1 use the same clock source):

0 = 50MHz

1 = 1MHz

0111 Start all / selected PWM as indicated by PWMCD

0 = start PWM selected with PWM2-0

1 = start all PWMs

Command 0x7F = start all PWMs.

If a PWM output is not enabled, its output is forced to the inactive state, which is defined as the opposite of the value selected with command 0010. The PWM may continue to run even though its output is disabled.

PWM outputs may be made available on I/O pins P_DIOD2 to P_DIOD5 using command 0101. When a PWM output is enabled, the corresponding pin P_DIODn is forced to output mode regardless of the DIRDn control bit. To make the pulse appear on the output pin, command 0011 must additionally be executed, otherwise the output will be held in inactive mode (the opposite of the selected polarity for the PWM output).

Please refer to Diamond Systems' Universal Driver 7.0 User Manual for information on using and programming the pulse width modulators.

8. WAVEFORM GENERATOR

The waveform generator includes a 2048 x 19 bit waveform buffer, which is organized as 16 bits of D/A data and a 3 bit channel tag. Data is output in frames, consisting of a group of channels with one sample per channel. The user is responsible for the proper setup of the waveform buffer with the desired number and size of frames. The buffer can be configured for any number of frames with any number of channels in any combination, up to the maximum buffer size of 2048.

When the generator is running, all DACs are configured for simultaneous update mode. Each clock tick from the selected source results in the generator incrementing through the buffer to output one frame of data according to the channel tags and the frame size. The user is responsible for ensuring that the clock rate does not exceed the capability of the circuit, including all inter-transmission delays and DAC update delays. Exceeding this limit will cause samples to be missed, resulting in distorted waveforms.

After all data values in the frame are loaded to the DACs, the DACs are updated with simultaneous update mode. When the last frame is output, if the generator is configured for one-shot operation it will stop, otherwise it will reset to the start of the buffer and continue. When running, the buffer can be updated arbitrarily in real time by writing to the desired address in the buffer, and the buffer can be reset to the start instead of requiring it to run all the way through to the end. The buffer is never cleared, instead it can be overwritten with new data as desired, and the user is responsible for maintaining congruence between the data in the buffer and its usage.

To load the waveform buffer, the user writes channel / data pairs to the buffer using registers 0, 1, 8, and 9. Writing to register 9 initiates the data load to the waveform buffer.

WGBA10-0 is the waveform buffer address, 0-0x7FF (2048 samples).

WGCH2-0 is the channel tag for the DA value at the selected address.

WGSRC1-0 is the clock source for frame incrementing:

WGSRC1	WGSRC0	Description
0	0	Manual (using WGINC command)
0	1	Counter 0 output
1	0	Counter 1 output
1	1	External trigger on DIO pin D0; this forces DIO port D0 to be input regardless of the setting in bit DIRD0

WGFR2-0: Frame size, 0-7; actual frame size is register value + 1

WGCYCLE: 0 = one shot, 1 = repetitive

WGFRC11-0: Frame count, 0-2047; actual size is register value + 1; frame count x frame size must be less than or equal to 2048 (max buffer size)

Command definitions

All commands take effect upon a 1 being written to the bit. In case of multiple 1s being written at the same time, the highest bit number is executed and the others are ignored.

WGINC	Software increment; output the current frame of data to the DACs; only works if clock source is set to software (WGSRC1-0 = 00)
WGRESET	Reset buffer address pointer to 0; The next frame output will be the first frame in the buffer; this command works both when the generator is running and when it is paused.
WGPAUSE	Stop waveform generator after the end of the current frame (if one is in progress)
WGSTART	Start waveform generator at the current buffer pointer location

Please refer to Diamond Systems' Universal Driver 7.0 User Manual for information on using and programming the waveform generator.

9. DIGITAL I/O OPERATION

Vega contains 30 3.3V digital I/O lines organized in four groups: A, B, C & D. Groups A to C consist of eight signals each and port D consist of only 6 signals. The direction of each port is independently programmable. All bits on all ports are individually programmable for input or output with register bits DIRA7-0, DIRB7-0, DIRD7-0, and DIRD7-0. A 0 means input mode and a 1 means output mode. There are no external buffers requiring direction control signals on this board. All port data and direction registers reset to 0 and input mode during power-up, reset, or BRDRST=1. If a port is in input mode, its output register may still be written to. When the port is switched to output mode, the value of the output register will drive the corresponding I/O pins.

Ports C and D also offer special pulse width modulator, waveform generator and counter/timer functions. This functionality supersedes the normal operation of these bits. When the special function is enabled, the port's direction is automatically changed to meet that function's requirements. The special function pin assignments and directions are shown below.

Port C bit	7	6	5	4	3	2	1	0
Special function	Ctr7 I/O	Ctr 6 I/O	Ctr 5 I/O	Ctr 4 I/O	Ctr 3 I/O	Ctr 2 I/O	Ctr 1 I/O	Ctr 0 I/O
Direction when enabled	Depends on selected function							

Port D bit	5	4	3	2	1	0
Special function	PWM3	PWM2	PWM1	PWM0	Waveform Trigger	A/D, User Int Trig
Direction when enabled	Out	Out	Out	Out	In	In

The port data are accessed at registers Base+8 through Base+10, and the port direction register is located at Base+11.

Base +	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
9	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
10	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
11	DIOCTR	-	-	DIRA	DIRCH	-	DIRB	DIRCL

The digital I/O lines are located at pins 1 through 24 on the connector J10. The lines are 3.3V and 5V logic compatible. Each output is capable of supplying –8mA in logic 1 state and +12mA in logic 0 state.

DIRA, DIRB, DIRCH, and DIRCL control the direction of ports A, B, C4-7 and C0-3. A direction value of 0 means output and 1 means input. All ports power up to input mode and the output registers are cleared to zero. When a port direction is changed to output, its output register is cleared to zero. When a port is in output mode, its value can be read back.

DIOCTR is used to control the function of lines C7-C4 on the I/O connector. When DIOCTR = 1, the lines are port C7-C4. When DIOCTR = 0, the lines are used for the counter/timer.

Pin No.	*DIOCTR = 1*	*DIOCTR = 0*	*Pin direction for DIOCTR = 0*
21	C4	Gate0	Input
22	C5	Gate1	Input
23	C6	Clk1	Input
24	C7	Out0	Output

Please refer to Diamond Systems' Universal Driver 7.0 User Manual for information on using and programming the digital I/O.

10. COUNTER/TIMER OPERATION

Vega offers eight 32-bit counter/timers with programmable functions. The counters are programmed using a command register at address 5 in the counter block, a counter number register at address 4, and a 32-bit data register CTRD31-0 at addresses 0-3.

Offset	7	6	5	4	3	2	1	0
5 (C)	CTRCMD3	CTRCMD2	CTRCMD1	CTRCMD0			CCD1	CCD0

0000 = Clear the selected counter. If count direction is up the counter register is cleared to 0. If count direction is down the counter register is set to the reload value. All other counter settings are preserved. If the counter is running it continues running.

0001 = Load the selected counter with data in registers 0-3. This is used for down counting operations only.

0010 = Select count direction. CCD0=1 means count up, and CCD0=0 means count down.

0011 = Enable / disable external gate. This command is not implemented in this design.

0100 = Enable / disable counting. CCD0 = 1 means enable counting, CCD0=0 means disable counting.

0101 = Latch selected counter. A counter must be latched before its contents can be read. Latching can occur while the counter is counting. The latched data is available in CTRD31-0.

0110 = Select counter clock source according to CCD1-0:

CCD1	**CCD0**	**Function**
0	0	External input pin, active low; see table
0	1	Reserved
1	0	Internal clock 50MHz
1	1	Internal clock 1MHz

If an external DIO pin is selected as the counter input, that DIO pin's direction is automatically set for input mode. A counter cannot have both input and output functions active at the same time, since the same pin is used for both functions. If both are selected, the input function will prevail.

0111 = Enable / disable Auto-Reload. CCD0 = 0 means disable auto-reload, CCD0 = 1 means enable auto-reload. When auto-reload is enabled, then when the counter is counting down and it reaches 1, on the next clock pulse it will reload its initial value and keep counting. Otherwise on the next clock pulse it will count down to 0 and stop.

1000 = Enable / disable counter output. This feature works only when the counter is counting down. If CCD1 = 1 then output is enabled, and if CCD1 = 0 then output is disabled. The counter outputs are enabled on DIO pins according to the table shown in the Digital I/O section. Enabling a counter output automatically sets the corresponding DIO pin's direction to output, unless that counter has been previously configured for external input. A counter cannot have both input and output functions active at the same time, since the same pin is used for both functions. If both are selected, the input function will prevail.

If CCD1 = 1 then CCD0 determines the output polarity. If CCD0 = 0 then the counter output is initially high. It will pulse low for one clock period whenever it reaches zero. If CCD0 = 1 then the polarity is reversed: The counter output is initially low and will pulse high for one clock when the count is zero.

1111 = Reset the counter. If CCD0 = 0, then only the counter specified in register 4 is reset. If CCD0 = 1 then all counters are reset. Reset means all registers and settings are cleared to zero. A command of 0xFF will reset all counters (although the precise command is 0xF1)..

Please refer to Diamond Systems' Universal Driver 7.0 User Manual for information on using and programming the counter/timers.

11. FLASHDISK MODULES

Vega is designed to accommodate an optional solid-state mSATA or USB flashdisk module. These modules contain up to 64GB of solid-state non-volatile memory that operates like a hard drive without requiring additional driver software support. Note that the mSATA flashdrive and PCIe MiniCard modules share the same socket. Only one of these module types may be used.

Model	*Capacity*	*Interface*
FDMM-64G-XT	64GB	mSATA MLC
FDMM-32G-XT	32GB	mSATA MLC
FDMM-16G-XT	16GB	mSATA MLC
FDMS-64G-XT	64GB	mSATA SLC
FDMS-32G-XT	32GB	mSATA SLC
FDMS-16G-XT	16GB	mSATA SLC
FDMS-8G-XT	8GB	mSATA SLC
FDU-1G-XT	1GB	USB
FDU-2G-XT	2GB	USB
FDU-4G-XT	4GB	USB
FDU-8G-XT	8GB	USB

USB Flashdisk Module

mSATA Flashdisk Module

11.1 Installing the Flashdisk Module

The flashdisk module installs directly on a connector and is held down with spacers and screws on a mounting hole on the board. For a USB flashdisk, this is connector J16 with one mounting spacer and screw. For a mSATA flashdisk, this is connector J27 with two mounting spacers and two screws.

12. SPECIFICATIONS

12.1 System

- Processor: 2.1GHz Intel Core i7-3612QE, 1.7GHz Intel Core i7-3517UE or 1.4GHz Intel Celeron 827E COM Express CPU module
- Cooling: Heat spreader with no fan
- SDRAM memory: Up to 8GB DDR3 SO-DIMMs
- Display type: VGA CRT, LCD LVDS, DisplayPort
- Supports dual independent displays
- CRT resolution: up to 2048 X 1536
- Flat panel resolution: UXGA 1600 X 1200
- USB ports: 4 USB 2.0
- Serial ports: 4 RS-232/422/485 up to 460.8kpbs
- Networking: 2 10/100/1000Mbps Ethernet
- Mass storage: 1 SATA pin header
- USB and mSATA solid state flashdisks of up to 64GB are supported
- Keyboard / mouse: USB
- Audio: HD audio with Realtek ALC262 CODEC; mic in, stereo in/out
- Expansion socket: PCIe MiniCard socket
- Bus interface: EMX (PCIe)
- +7-36V DC/DC on-board power supply
- Power consumption: VEGA-3612QE-4GA -- 14.52W at 12V typical
  VEGA-3517UE-4GA -- 13.93W at 12V typical
  VEGA-827E-2GA -- 14.7W at 12V typical

12.2 Data Acquisition

- 16 16-bit analog inputs
- Inputs user-configurable as: 16 single-ended, 8 differential, or 16 SE + 8 DI
- Bipolar ranges: ±10V, ±5V, ±2.5V, ±1.25V
- Unipolar ranges: 0-10V, 0-5V, 0-2.5V
- Conversion rate: 250KHz aggregated A/D sampling rate for gains below 4
  100KHz aggregated A/D sampling rate for gains 4 and 8
- FIFO: 2048 samples, programmable threshold
- Accuracy < ±2 LSB, after calibration
- Nonlinearity: ±3LSB, no missing codes
- Input bias current: 100pA max
- Input Impedance: 10^13 ohms
- Protection: ±35V on any analog input without damage
- A/D and D/A calibration: on-board I2C flash EEPROM for storage of auto-calibration values
- 8 16-bit analog outputs
- Output ranges: ±10V, 0-10V
- Output current: ±5mA max per channel, 2KΩ min load
- Settling time: 7µS to ±0.01%
- Relative accuracy: ±1 LSB
- Nonlinearity: ±1 LSB, monotonic
- Reset: Reset to zero-scale or mid-scale (jumper selectable)
- Indefinite short circuit protection on outputs
- 30 digital I/O lines arranged in four groups (A, B, C, and D)
- Input logic thresholds :
  Logic 0: 0.0V min, 0.8V max
  Logic 1: 2.0V min, 5.0V max
- Input current: ±1µA max
- Output logic thresholds:
  Logic 0: 0.0V min, 0.33V max
  Logic 1: 2.4V min, 3.3V max
- Output current:
  Logic 0: 12mA max per line
  Logic 1: -4mA max per line

- 4 24-bit pulse width modulators
- 8-channel waveform generator

12.3 Mechanical & Environmental

- Operating temperature: -40°C to +85°C
- Shock: MIL-STD-202G, Method 213B compatible
- Vibration: MIL-STD-202G, Method 214A compatible
- Dimensions: Vega Core i-7 models -- 4.92" x 3.74" x 1.4" (125mm x 95mm x 35.7mm)
- MTBF: Vega baseboard with DAQ – 277,880 hours @ 20°C
  Core i7-3612QE & Core i7-3517UE COMs – 146,217 hours at 25°C
  Celeron 827E COM – 187,678 hours at 25°C
- RoHS: Compliant